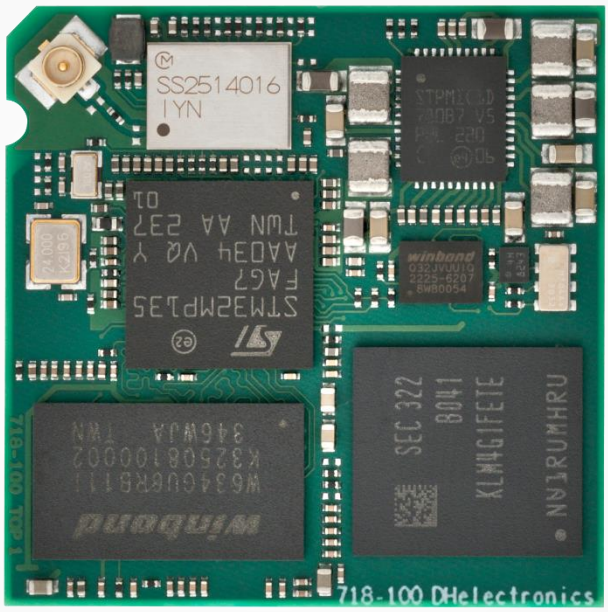
DHCOR STM32MP13

User manual



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History

Version	Data	Description of changes	Name
R01	12.02.2024	First draft	AG
R01	13.06.2024	Review and released	MA

1 Index of Contents

2 Abbreviations

- ANA = Analog
- BGA = Ball grid array
- CLK = Clock
- DNC = Do not connect
- EMC = Electro magnetic compatibility
- ESD = electrostatic discharge
- EXTI = Extended interrupt and event controller
- FPS = Frames per second
- HW = Hardware
- I/O = Input/output
- LGA = Land grid array
- MBC = Must be connected
- MSL = Moisture sensitivity level
- Msps = Mega samples per second
- NC = No connect
- OE = Open Embedded
- PD = Pull-down
- PnP = Pick and place
- PU = Pull-up
- RFU = Reserve for Future Use
- RH = Relative humidity
- RST = Reset
- SAC = SnAgCu (Tin-silver-copper)
- SMT = Surface mounted technology
- SSU = Should stay connected
- SWD = Serial wire debug
- TBD = To be defined
- VSF = Vendor specific function

3 Introduction

3.1 Hardware

The DHCOR-STM32MP13-01LG is a solderable computer module with a footprint of 29 x 29 mm². The space-saving module increases operational safety through direct soldering and saves space- and cost-intensive board-to-board connectors. The DHCOR STM32MP13 can be equipped with processors of the new STM32MP13 family and contains a single Cortex-A7 core (up to 1 GHz).

The module from the STM32MP13 family provides many embedded interfaces such as two 12 bit ADCs, PWM/Timer, 135 GPIO, UART, SPI, RTC, up to 2x FD CAN and standard features like I2S, I2C™, two times Gbit Ethernet, 8, 10 or 16 bit camera interface, SD/MMC and one each USB 2.0 High Speed OTG and host port. The display interface is a 24 bit RGB connection with HD resolution (1920 x 1080 pixels @ 30fps).

The DHCOR STM32MP13 is perfectly suited for many fields of application and sets itself apart from the masses with its cost optimized Linux capabilities. The STM32MP13 family enables powerful IoT and/or HMI applications from sensors and actuators to the cloud with just one chip.

3.2 Software

Currently, the DHCOR-STM32MP13-01LG module is available with the Embedded Linux operating system based on OE/Yocto based. In addition, the DHSBC STM32MP13 reference design is also up streamed to mainline Linux and U-Boot. And the SOM is also maintained over the years based on this board.

3.3 Main characteristics

- Single Cortex®-A7 up to 1 GHz
- Power efficient and cost optimized application processor
- Power management: STPMIC1D
- Crypto Engine, Secure Boot
- Quad SPI boot flash: 4 MByte
- DDR3 memory (16 bit): 128 - 512 MByte
- Bus interface: 8 / 16 Bit address / data
- Ethernet: 2x Gbit, IEEE 1588v2, 2x MDIO
- MMC/SD: 2x SDIO 4.0 / SD 4.1 / eMMC 4.51
- NAND: 8 / 16 Bit interface Raw MLC / SLC, 4 or 8 Bit ECC
- CAN: 2x FDCAN / 1x TTCAN
- UART: 4x UART, 4x USART up to 12.5 MBit/s

- SPI: 5x up to 50 MBit/s
- I2C™: 5x
- USB Host: 1x USB 2.0 HS
- USB OTG: 1x OTG 2.0 HS
- Embedded USB PHYs: 2x
- CSI (parallel camera): 1x 8 to 16 Bit / pixel data format
- Display RGB: Max. Full HD 1920 x 1080 pixels @ 30 fps, 24 Bit
- ADC: 2x 12-Bit max. resolution up to 5 Msps
- Temperature sensor: 1x
- SPDIF: 4x Rx
- I2S / SAI: 2x
- GPIOs: 135x
- PWM / Timer:
    - 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
    - 2× 16-bit advanced timers
    - 10× 16-bit general-purpose timers (including 2 basic timers without PWM)
    - 5× 16-bit low-power timers
    - 4 Cortex®-A7 system timers (secure, non-secure, virtual, hypervisor)
    - 2× independent watchdogs
- RTC: Secure RTC with sub-second accuracy and hardware calendar
- DFSDM: 1x with 4 channels / 2 filters
- Hardware acceleration:
    - AES 128, 192, 256 DES/TDES
    - AES 128, 256 with DPA protection
    - PKA ECC/RSA with DPA protection
    - AES 128 on-the-fly DRAM encryption and decryption
    - HASH (SHA-1, SHA-224, SHA-256, SHA-384,
    - SHA-512, SHA-3), HMAC
    - 1x true random number generator (6 triple oscillators)
    - 1x CRC calculation unit
- Debug interface: JTAG interface
- Industrial temperature range (-40°C to +85°C)

3.4 Further technical information

Beside this manual, please also have a look at the ST application note **AN5474** "**Getting started with STM32MP13 series hardware development**". This document shows how to use the STM32MP13 series and describes the minimum hardware resources required to develop a carrier board based on those MPU products.

3.4.1 STM32MP13 processor

Data sheets and technical documents can be found at
https://wiki.st.com/stm32mpu/wiki/STM32MP13_resources

3.4.2 STPMIC1 power manager

Data sheets and technical documents can be found at
https://wiki.st.com/stm32mpu/wiki/STM32MP13_resources

3.4.3 RV-3032-C7 real time clock

Data sheets and technical documents can be found at https://www.microcrystal.com/en/products/real-time-clock-rtc-modules/rv-3032-c7/

3.4.4 1YN Wi-Fi®/Bluetooth module

Data sheets and technical documents can be found at https://www.murata.com/en-eu/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type1yn

3.4.5 M24256E EEPROM

Data sheets and technical documents can be found at https://www.st.com/en/memories/m24256e-f.html

4 Hardware overview

4.1 Block diagram

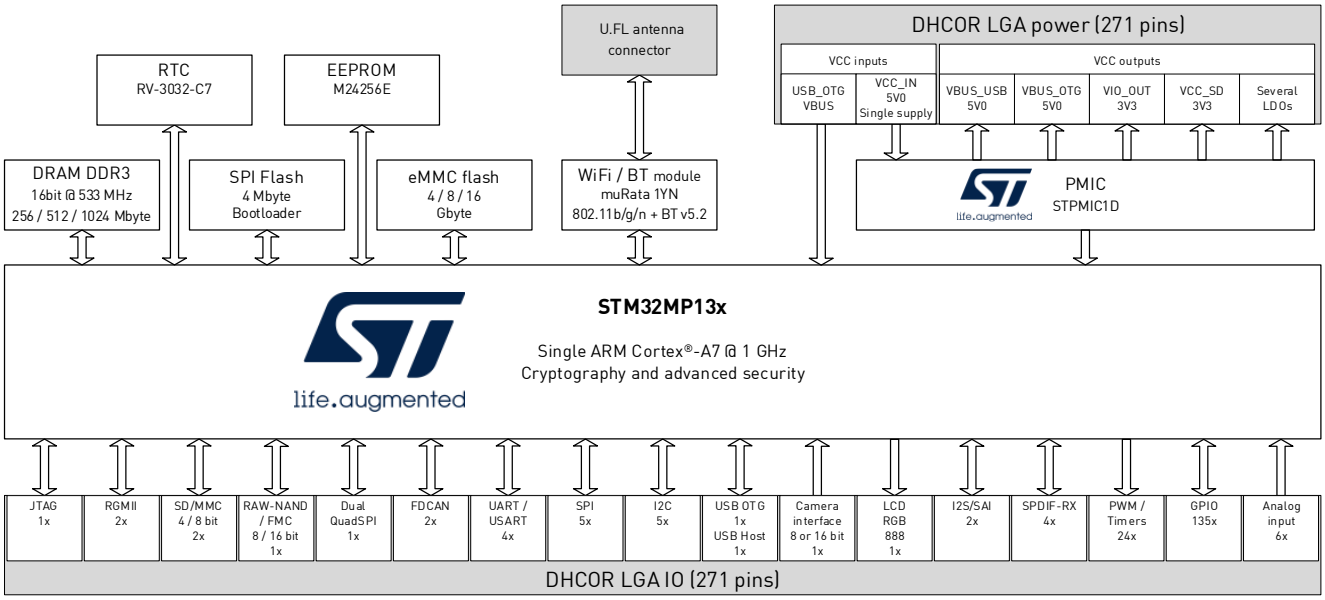


Figure 1: DHCOR-STM32MP13-01LG block diagram

4.2 Configuration overview

DHCR-CPU-Cxxx-Rxxx-EE[-Fxxxx][-SPI][-RTC][-WBT]-X-01LG	
CPU	STM32MP135F: Single Cortex®-A7 with 1 GHz, HW Crypto, Display + Camera, FDCAN, 2x Ethernet, 2x ADC STM32MP135C: Single Cortex®-A7 with 650 MHz, HW Crypto, Display + Camera, FDCAN, 2x Ethernet, 2x ADC STM32MP131C: Single Cortex®-A7 with 650 MHz, HW Crypto, 1x Ethernet, 1x ADC (Please contact us for other options like STM32MP133)
Cxxx	650 MHz: C065, 1 GHz: C100
Rxxx	128 Mbyte: R012, 256 Mbyte: R025, 512 Mbyte: R051 , 1024 Mbyte: R102
EE	256 kbit EEPROM
X	Commercial temperature range (0 °C - 70 °C): C, Industrial temperature range (-40 °C - 85 °C): I (only -30 - 70 °C with option WBT) Note: Industrial temp. range for eMMC version is -25 °C - 85 °C. Please contact us for -40 °C - 85 °C version.
01LG	DHCOR Revision, LGA connection
Options	
[-Fxxxx]	4096 Mbyte eMMC: F0409, 8192 Mbyte eMMC: F0819, 16384 Mbyte eMMC: F1638
[-SPI4]	4 Mbyte SPI boot flash
[-RTC]	Low power temperature compensated real time clock (instead of CPU internal RTC)
[-WBT]	WiFi and Bluetooth® via Murata 1YN module with U.FL connector: WBT

Table 1: Model number for ordering

Our standard product is defined as follows: **DHCR-STM32MP135F-C100-R051-EE-F0409-SPI4-RTC-WBT-I-01LG**

Other configurations on request.

4.2.1 SDMMC variant overview

The STM32MP13 has only 2 SDMMC interfaces. eMMC and WiFi are connected via SDMMC, therefore the availability of an external SDMMC interface depends on the configuration. The following figure shows the possible configurations.

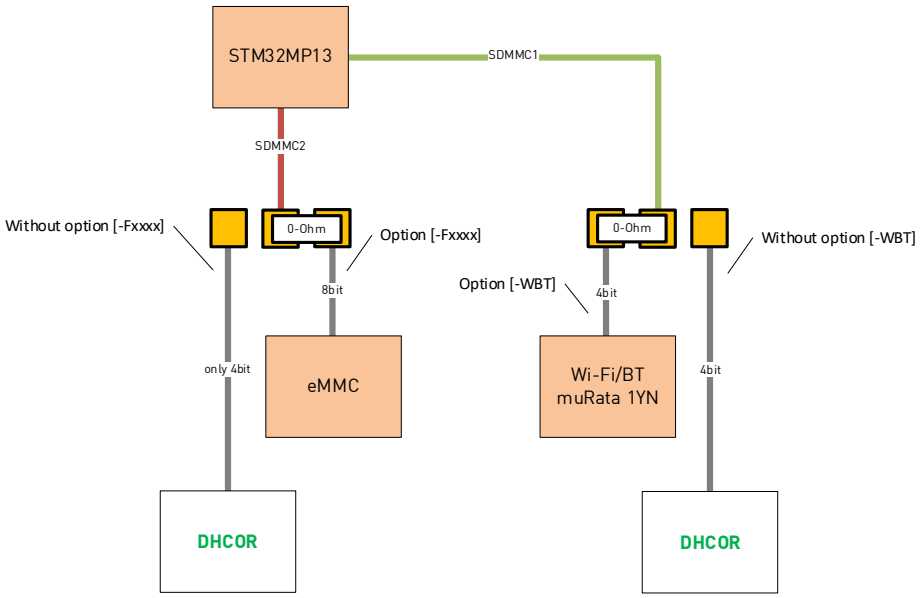


Figure 2: SDMMC connection

4.2.2 Bluetooth-UART variant overview

On a System-On-Module with WiFi/BT, the UART7 is used for the Bluetooth connection and is not available for external use.

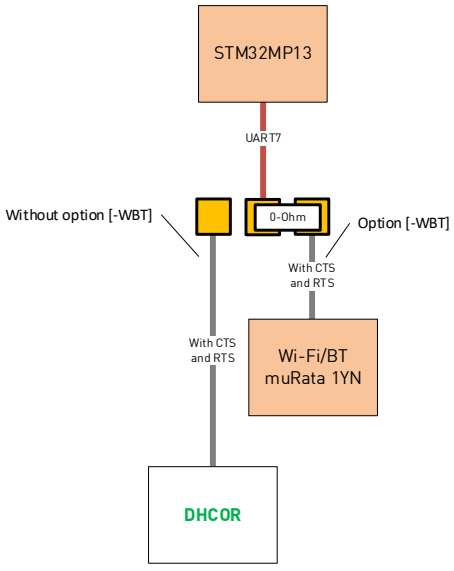


Figure 3: Bluetooth UART

4.3 DHCOR STM32MP13 Development Board

The reference design for DHCOR STM32MP13 is the DHCOR STM32MP13 Development Board:

Links tbd...

Important: It is recommended to reuse the DHCOR pin assignment of the Development Board as far as possible in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can be taken from the Development Board, without any BSP porting efforts.

4.4 Pin-Mux example configurations

The DHCOR STM32MP13 Development Board only provides a headless reference implementation. Therefore, DH electronics also provides a default configuration for the DHCOR STM32MP13 for display applications. The next table shows an overview about all interfaces for both available configurations. Differences are marked with blue.

DHCOR STM32MP13 **Development Board configuration** **Note:** Marked **"headless"** in the document	**HMI example configuration** **Note:** Marked **"HMI"** in the document
2x SPI	1x SPI
1x Quad SPI (used for SPI NOR flash on the SOM)	1x Quad SPI (used for SPI NOR flash on the SOM)
2x UART with CTS/RTX (with Bluetooth only 1x available)	2x UART with CTS/RTX (with Bluetooth only 1x available)
1x UART only TX/RX	-
1x Serial console UART	1x Serial console UART
3x I2C (2x free for use, 1x used on SOM for PMIC, ...)	3x I2C (2x free for use, 1x used on SOM for PMIC, ...)
2x FDCAN	2x FDCAN
2x SDMMC (used for eMMC and WiFi on the SOM)	2x SDMMC (used for eMMC and WiFi on the SOM)
1x SAI	1x SAI
2x 1Gbit Ethernet	2x 100Mbit Ethernet
1x USB Host	1x USB Host
1x USB OTG	1x USB OTG
3x ADC input	3x ADC input
2x PWM (TIM)	2x PWM (TIM)
1x JTAG	1x JTAG
14x GPIO free for use	9x GPIO free for use
-	1x 24bit RGB display interface

Table 2: Pin-Mux example configurations

The CubeMx and pin-Mux Files are available here: Links tbd...

4.5 Pin assignment

The DHCOR-STM32MP13-01LG comes with the CPU type STM32MP13xxAG7 and with 9 x 9 mm TFBGA289 package.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
PC12	SDMMC1_CK	A2	GPIO	I/O	PC12	B13	Only available without WiFi/BT	-
PD2	SDMMC1_CMD	A3	GPIO	I/O	PD2	G11	Only available without WiFi/BT	-
PC11	SDMMC1_D3	A4	GPIO	I/O	PC11	C12	Only available without WiFi/BT	-
PC8	SDMMC1_D0	A5	GPIO	I/O	PC8	C13	Only available without WiFi/BT	-
PC9	SDMMC1_D1	A6	GPIO	I/O	PC9	G12	Only available without WiFi/BT	-
PC10	SDMMC1_D2	A7	GPIO	I/O	PC10	F11	Only available without WiFi/BT	-
NC	Not connected	A8	-	-	-	-	-	-
GND	GND	A29	PWR	-	-	-	-	MBC
VCC_IO[2]	PMIC: 1V8 or 3V3	A10	PWR	Output	-	-	-	-
WL_GPIO_2[3]	1YN: WL_GPIO_2	A11	GPIO	I/O	-	-	Only available with WiFi/BT	-
PG10	FDCAN1_TX	A12	GPIO	I/O	PG10	H2	-	-
PD0	FDCAN1_RX	A13	GPIO	I/O	PD0	E1	-	-
PD8	UART4_RX	A14	GPIO	I/O	PD8	B2	Serial console UART	-
PA9	UART4_TX	A15	GPIO	I/O	PA9	D2	Serial console UART	-
PI2	BT_REG_ON_PI2	A16	GPIO	I/O	PI2	J4	Used for Bluetooth REG_ON. DNC if WiFi/BT is mounted.	-
PE12	Headless: SPI2_PIRQ HMI: LTDC_G6	A17	GPIO	I/O	PE12	B1	-	-
PONKEYn[4]	PMIC: PONKEYn	A18	GPIO	Input	-	-	Connected to PMIC	-
VBUS_OTG[5]	PMIC: VBUS_OTG	A19	PWR	Output	-	-	Connected to PMIC	-
VCC_IN_5V	5V supply voltage	A20	PWR	Input	-	-	-	MBC
VCC_IN_5V	5V supply voltage	A21	PWR	Input	-	-	-	MBC
PA2	ETH1_MDIO	B1	GPIO	I/O	PA2	R5	-	-
GND	GND	B2	PWR	-	-	-	-	MBC
GND	GND	B3	PWR	-	-	-	-	MBC
GND	GND	B4	PWR	-	-	-	-	MBC
GND	GND	B5	PWR	-	-	-	-	MBC
GND	GND	B6	PWR	-	-	-	-	MBC

[1] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".
[2] Connected to STPMIC1D Pin 31. BUCK3 output voltage. For more information see STPMIC1D datasheet.
[3] This pin is connected to the WiFi/BT module 1YN Pin 17. For more information see muRata 1YN datasheet.
[4] Connected to STPMIC1D Pin 17. User Power ON Key (active low with internal pullup).
[5] These pins are connected to STPMIC1D Pin 35. USB OTG power output switch. For more information see STPMIC1D datasheet.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
GND	GND	B7	PWR	-	-	-	-	MBC
GND	GND	B8	PWR	-	-	-	-	MBC
GND	GND	B9	PWR	-	-	-	-	MBC
GND	GND	B10	PWR	-	-	-	-	MBC
GND	GND	B11	PWR	-	-	-	-	MBC
GND	GND	B12	PWR	-	-	-	-	MBC
GND	GND	B13	PWR	-	-	-	-	MBC
GND	GND	B14	PWR	-	-	-	-	MBC
GND	GND	B15	PWR	-	-	-	-	MBC
GND	GND	B16	PWR	-	-	-	-	MBC
GND	GND	B17	PWR	-	-	-	-	MBC
GND	GND	B18	PWR	-	-	-	-	MBC
GND	GND	B19	PWR	-	-	-	-	MBC
GND	GND	B20	PWR	-	-	-	-	MBC
VCC_IN_5V	5V supply voltage	B21	PWR	Input	-	-	-	MBC
PG2	ETH1_MDC	C1	GPIO	I/O	PG2	U3	-	-
GND	GND	C2	PWR	-	-	-	-	MBC
PA3	ADC1_INP12	C3	GPIO	I/O	PA3	T7	-	-
NC	Not connected	C4	-	-	-	-	-	-
LPO_IN_32kHz[6]	1YN: LPO_IN_32kHz	C5	CLK	Input	-	-	Used for WiFi/BT ref. clock. Connect 32kHz oscillator if WiFi/BT is mounted.	MBC
PE4	Headless: DFSDM1_DATIN3 HMI: SAI1_FS_A	C6	GPIO	I/O	PE4	K1	-	-
PF12	WL_REG_ON_PF12	C7	GPIO	I/O	PF12	J9	Used for WiFi REG_ON. DNC if WiFi/BT is mounted.	-
NC	Not connected	C8	-	-	-	-	-	-
PH8	Headless: PH8 HMI: USART2_RX	C9	GPIO	I/O	PH8	F1	-	-
WL_GPIO_1[7]	1YN: WL_GPIO_1	C10	GPIO	I/O	-	-	Only available with WiFi/BT	-
VBAT_WIFI[8]	1YN: VBAT_WIFI	C11	PWR	Input	-	-	Only available with WiFi/BT. Do not connect this pin.	DNC
LDO6_OUT[9]	PMIC: LDO6_OUT	C12	PWR	Output	-	-	-	-
VCC_IO[10]	PMIC: 1V8 or 3V3	C13	PWR	Output	-	-	-	-
GND	GND	C14	PWR	-	-	-	-	MBC
LDO2_OUT[11]	PMIC: LDO2_OUT	C15	PWR	Output	-	-	-	-

[6] This pin is connected to the WiFi/BT module 1YN Pin 37. This pin must be connected to an external 32kHz oscillator, if the WiFi/BT module 1YN is mounted. For more information see muRata 1YN datasheet.
[7] This pin is connected to the WiFi/BT module 1YN Pin 18. For more information see muRata 1YN datasheet.
[8] This pin is connected to the WiFi/BT module 1YN Pin 30. No external supply voltage is needed, because with default mounting option, this voltage is supplied internal. For more information see muRata 1YN datasheet.
[9] Connected to STPMIC1D Pin 21. LDO6 output voltage. For more information see STPMIC1D datasheet.
[10] Connected to STPMIC1D Pin 31. BUCK3 output voltage. For more information see STPMIC1D datasheet.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
LDO5_OUT[12]	PMIC: LDO5_OUT	C16	PWR	Output	-	-	-	-
LDO3_OUT[13]	PMIC: LDO3_OUT	C17	PWR	Output	-	-	-	-
SW_OUT[14]	PMIC: SW_OUT	C18	PWR	Output	-	-	-	-
PE13	Headless: I2C5_SDA HMI: LTDC_R6	C19	GPIO	I/O	PE13	C1	-	-
GND	GND	C20	PWR	-	-	-	-	MBC
PG8	#ETH2_RST	C21	GPIO	I/O	PG8	J3	-	-
PD7	Headless: ETH1_RXC HMI: PD7	D1	GPIO	I/O	PD7	R3	-	-
GND	GND	D2	PWR	-	-	-	-	MBC
VCC_IO[15]	PMIC: 1V8 or 3V3	D3	PWR	Output	-	-	-	-
BT_PCM_SYNC [16]	1YN: BT_PCM_SYNC	D4	GPIO	I/O	-	-	Only available with WiFi/BT	-
PA5	USB_PWR_CC1	D5	GPIO	I/O	PA5	M7	-	-
PE14	WL_HOST_WAKE	D6	GPIO	I/O	PE14	E2	Used as WiFi HOST_WAKE signal. DNC if WiFi/BT is mounted.	-
PH2	UART7_TX	D7	GPIO	I/O	PH2	G2	Only available without WiFi/BT	-
PE10	UART7_RX	D8	GPIO	I/O	PE10	C7	Only available without WiFi/BT	-
PB12	UART7_RTS	D9	GPIO	I/O	PB12	A7	Only available without WiFi/BT	-
PG7	UART7_CTS	D10	GPIO	I/O	PG7	C8	Only available without WiFi/BT	-
NC	Not connected	D11	-	-	-	-	-	-
PD3	Headless: DFSDM1_CKOUT HMI: USART2_CTS	D12	GPIO	I/O	PD3	G6	-	-
PG9	BT_DEV_WAKE	D13	GPIO	I/O	PG9	G5	Used as Bluetooth DEVICE_WAKE signal. DNC if WiFi/BT is mounted.	-
PD13	Headless: Mainboard-HW-CODING_1 and PD13 HMI: Mainboard-HW-CODING_1 and LTDC_G4	D14	GPIO	I/O	PD13	N1	-	-
PH3	Headless: Mainboard-HW-CODING_0 and PH3 HMI: Mainboard-HW-	D15	GPIO	I/O	PH3	T2	-	-

[11] Connected to STPMIC1D Pin 18. LDO2 output voltage. For more information see STPMIC1D datasheet.
[12] Connected to STPMIC1D Pin 20. LDO5 output voltage. For more information see STPMIC1D datasheet.
[13] Connected to STPMIC1D Pin 14. LDO3 output voltage. For more information see STPMIC1D datasheet.
[14] Connected to STPMIC1D Pin 38. SW_OUT output voltage. For more information see STPMIC1D datasheet.
[15] Connected to STPMIC1D Pin 31. BUCK3 output voltage. For more information see STPMIC1D datasheet.
[16] This pin is connected to the WiFi/BT module 1YN Pin 8. For more information see muRata 1YN datasheet.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
	CODING_0 and LTDC_B4							
PF5	Headless: PF5 HMI: LTDC_G0	D16	GPIO	I/O	PF5	D1	-	-
PD10	Headless: PD10 HMI: LTDC_B2	D17	GPIO	I/O	PD10	D3	-	-
PE1	Headless: PE1 HMI: LTDC_HSYNC	D18	GPIO	I/O	PE1	C3	-	-
PD1	I2C5_SCL	D19	GPIO	I/O	PD1	C2	-	-
GND	GND	D20	PWR	-	-	-	-	MBC
PG15	ETH2_INTB	D21	GPIO	I/O	PG15	G8	-	-
PA7	Headless: ETH1_RXCTL HMI: ETH1_CRS_DV	E1	GPIO	I/O	PA7	R6	-	-
GND	GND	E2	PWR	-	-	-	-	MBC
PF13	USB_PWR_CC2	E3	GPIO	I/O	PF13	T3	-	-
BT_PCM_IN[17]	1YN: BT_PCM_IN	E4	GPIO	Input	-	-	Only available with WiFi/BT	-
PC4	ETH1_RXD0	F1	GPIO	I/O	PC4	K9	-	-
GND	GND	F2	PWR	-	-	-	-	MBC
PWR_CPU_ON	PWR_CPU_ON	F3	GPIO	Output	PWR_CPU_ON	R4	-	-
BT_PCM_OUT[18]	1YN: BT_PCM_OUT	F4	GPIO	Output	-	-	Only available with WiFi/BT	-
PC5	ETH1_RXD1	G1	GPIO	I/O	PC5	P8	-	-
GND	GND	G2	PWR	-	-	-	-	MBC
PC3	ADC1_IN	G3	GPIO	I/O	PC3	P7	-	-
BT_PCM_CLK[19]	1YN: BT_PCM_CLK	G4	GPIO	I/O	-	-	Only available with WiFi/BT	-
PB0	Headless: ETH1_RXD2 HMI: PB0	H1	GPIO	I/O	PB0	M8	-	-
GND	GND	H2	PWR	-	-	-	-	MBC
VREF+	VREF+	H3	PWR	Input	VREF+	U6	By default, VREF+ is supplied from PMIC LDO1_OUT = 1V8. DNC	-
PC0	Headless: USART1_TX HMI: PC0	H4	GPIO	I/O	PC0	T4	-	-
PB1	Headless: ETH1_RXD3 HMI: PB1	J1	GPIO	I/O	PB1	N8	-	-
GND	GND	J2	PWR	-	-	-	-	MBC
PF14	DEBUG_JTCK-SWCLK	J3	GPIO	I/O	PF14	U4	-	-
PA13	HW-CODING_0	J4	GPIO	I/O	PA13	K7	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.	-

[17] This pin is connected to the WiFi/BT module 1YN Pin 9. For more information see muRata 1YN datasheet.
[18] This pin is connected to the WiFi/BT module 1YN Pin 10. For more information see muRata 1YN datasheet.
[19] This pin is connected to the WiFi/BT module 1YN Pin 11. For more information see muRata 1YN datasheet.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
USB_D1_M	USB_D1_M	K1	USB	Analog	USB_D1_M	U12	-	-
GND	GND	K2	PWR	-	-	-	-	MBC
PI7	OTG_HS_VBUS	K3	GPIO	I/O	PI7	U13	-	-
PI1	HW-CODING_1	K4	GPIO	I/O	PI1	N4	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.	-
USB_D1_P	USB_D1_P	L1	USB	Analog	USB_D1_P	T12	-	-
GND	GND	L2	PWR	-	-	-	-	MBC
PA10	PA10	L3	GPIO	I/O	PA10	J12	-	-
PH12	TIM5_CH3	L4	GPIO	I/O	PH12	G7	-	-
USB_D2_M	USB_D2_M	M1	USB	Analog	USB_D2_M	U9	-	-
GND	GND	M2	PWR	-	-	-	-	MBC
PH4	DEBUG_JTDI	M3	GPIO	I/O	PH4	T13	-	-
PA6	TIM13_CH1	M4	GPIO	I/O	PA6	R8	-	-
USB_D2_P	USB_D2_P	N1	USB	Analog	USB_D2_P	T9	-	-
GND	GND	N2	PWR	-	-	-	-	MBC
PWR_LP	PWR_LP	N3	GPIO	Output	PWR_LP	U14	-	-
PF15	DEBUG_JTMS-SWDIO	N4	GPIO	I/O	PF15	L10	-	-
PB11	Headless: ETH1_TXCTL HMI: ETH1_TX_EN	P1	GPIO	I/O	PB11	M6	-	-
GND	GND	P2	PWR	-	-	-	-	MBC
NC	Not connected	P3	-	-	-	-	-	-
DEBUG_JTRST	DEBUG_JTRST	P4	GPIO	Input	NJTRST	R10	-	-
PC1	Headless: ETH1_TXC HMI: PC1	R1	GPIO	I/O	PC1	R7	-	-
GND	GND	R2	PWR	-	-	-	-	MBC
NC	Not connected	R3	-	-	-	-	-	-
PH5	DEBUG_JTDO-SWO	R4	GPIO	I/O	PH5	L12	-	-
PE5	Headless: ETH1_TXD3 HMI: PE5	T1	GPIO	I/O	PE5	L9	-	-
GND	GND	T2	PWR	-	-	-	-	MBC
NC	Not connected	T3	-	-	-	-	-	-
PA14	MCO_2	T4	GPIO	I/O	PA14	R11	-	-
PC2	Headless: ETH1_TXD2 HMI: PC2	U1	GPIO	I/O	PC2	U8	-	-
GND	GND	U2	PWR	-	-	-	-	MBC
NC	Not connected	U3	-	-	-	-	-	-
NC	Not connected	U4	-	-	-	-	-	-
PD4	Headless: SPI3_MISO HMI: LTDC_R1	E18	GPIO	I/O	PD4	A2	-	-
PE0	Headless: FDCAN2_RX HMI: LTDC_B1	E19	GPIO	I/O	PE0	B3	-	-
GND	GND	E20	PWR	-	-	-	-	MBC
PF7	ETH2_TXD0	E21	GPIO	I/O	PF7	J7	-	-

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
PE11	Headless: SAI1_FS_A HMI: LTDC_R0	F18	GPIO	I/O	PE11	E4	-	-
PG0	Headless: FDCAN2_TX HMI: LTDC_G5	F19	GPIO	I/O	PG0	A4	-	-
GND	GND	F20	PWR	-	-	-	-	MBC
PG11	ETH2_TXD1	F21	GPIO	I/O	PG11	R1	-	-
PA15	Headless: Mainboard-HW-CODING_2 and PA15 HMI: Mainboard-HW-CODING_2 and LTDC_G7	G18	GPIO	I/O	PA15	E7	-	-
PH7	QUADSPI_BK1_IO3	G19	GPIO	I/O	PH7	L3	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
GND	GND	G20	PWR	-	-	-	-	MBC
PG1	Headless: ETH2_TXD2 HMI: SPI2_MISO	G21	GPIO	I/O	PG1	P4	-	-
PG4	Headless: PG4 HMI: LTDC_VSYNC	H18	GPIO	I/O	PG4	C9	-	-
PF9	QUADSPI_BK1_IO1	H19	GPIO	I/O	PF9	H9	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
GND	GND	H20	PWR	-	-	-	-	MBC
PE6	Headless: ETH2_TXD3 HMI: LTDC_G3	H21	GPIO	I/O	PE6	R2	-	-
PB2	QUADSPI_BK1_NCS	J18	GPIO	I/O	PB2	K3	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
PF10	QUADSPI_CLK	J19	GPIO	I/O	PF10	K2	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
GND	GND	J20	PWR	-	-	-	-	MBC
PG3	Headless: ETH2_TXC HMI: FDCAN2_RX	J21	GPIO	I/O	PG3	U2	-	-
CLKOUT[20]	RTC: CLKOUT	K18	GPIO	Output	-	-	-	-

[20] This pin is connected to the RTC RV-3032-C7 Pin 7. For more information see MicroCrystal datasheet.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
PF8	QUADSPI_BK1_IO0	K19	GPIO	I/O	PF8	H3	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
GND	GND	K20	PWR	-	-	-	-	MBC
PF6	Headless: ETH2_TXCTL HMI: ETH2_TX_EN	K21	GPIO	I/O	PF6	L1		-
RTC_EVI[21]	RTC: RTC_EVI	L18	GPIO	Input	-	-	-	-
PD11	QUADSPI_BK1_IO2	L19	GPIO	I/O	PD11	G1	Connected to the SPI Flash on the SOM. Can only be used with the eMMC boot SOM variant w/o SPI flash.	-
GND	GND	L20	PWR	-	-	-	-	MBC
PA8	Headless: ETH2_RXD3 HMI: SPI2_MOSI	L21	GPIO	I/O	PA8	J8	-	-
PI0[22]	PI0 and RTC: RTC_#INT	M18	GPIO	I/O	PI0	N3	-	-
PE9	Headless: SPI2_RST HMI: LTDC_R7	M19	GPIO	I/O	PE9	A3	-	-
GND	GND	M20	PWR	-	-	-	-	MBC
PH6	Headless: ETH2_RXD2 HMI: SPI2_SCK	M21	GPIO	I/O	PH6	J6	-	-
PD14	Headless: TIM4_CH3 HMI: LTDC_R4	N18	GPIO	I/O	PD14	F7	-	-
PE7	Headless: PE7 HMI: LTDC_R5	N19	GPIO	I/O	PE7	C4	-	-
GND	GND	N20	PWR	-	-	-	-	MBC
PE2	ETH2_RXD1	N21	GPIO	I/O	PE2	T1	-	-
PA0	SAI1_SD_B	P18	GPIO	I/O	PA0	L7	-	-
PD15	Headless: USART2_RX HMI: LTDC_B5	P19	GPIO	I/O	PD15	A5	-	-
GND	GND	P20	PWR	-	-	-	-	MBC
PF4	ETH2_RXD0	P21	GPIO	I/O	PF4	P3	-	-
PF1	Headless: SPI3_MOSI HMI: LTDC_G1	R18	GPIO	I/O	PF1	A8	-	-
PB7	BT_HOST_WAKE	R19	GPIO	I/O	PB7	D5	Used as Bluetooth HOST_WAKE signal. DNC if WiFi/BT is mounted.	-
GND	GND	R20	PWR	-	-	-	-	MBC
PA12	Headless: ETH2_RXCTL	R21	GPIO	I/O	PA12	F2	-	-

[21] This pin is connected to the RTC RV-3032-C7 Pin 4. For more information see MicroCrystal datasheet.
[22] This pin is connected to the RTC RV-3032-C7 Pin 3 and to STM32MP13 IO PI0. For more information see also MicroCrystal datasheet. If RTC RV-3032-C7 is not mounted pin PI0 is free for use, otherwise the pin is used as RTC interrupt.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
	HMI: ETH2_CRS_DV							
PA4	SAI1_SCK_A	T18	GPIO	I/O	PA4	N7	-	-
PE15	Headless: USART2_CTS HMI: LTDC_B7	T19	GPIO	I/O	PE15	A6	-	-
GND	GND	T20	PWR	-	-	-	-	MBC
PH11	Headless: ETH2_RXC HMI: SPI2_NSS	T21	GPIO	I/O	PH11	H7	-	-
PD6	SAI1_SD_A	U18	GPIO	I/O	PD6	G9	-	-
PF2	Headless: #USB_PWR_FLT HMI: LTDC_B3	U19	GPIO	I/O	PF2	B7	-	-
GND	GND	U20	PWR	-	-	-	-	MBC
PG5	ETH2_MDC	U21	GPIO	I/O	PG5	H1	-	-
PG14	ETH1_TXD1	V1	GPIO	I/O	PG14	T8	-	-
GND	GND	V2	PWR	-	-	-	-	MBC
NC	Not connected	V3	-	-	-	-	-	-
NC	Not connected	V4	-	-	-	-	-	-
NC	Not connected	V5	-	-	-	-	-	-
NC	Not connected	V6	-	-	-	-	-	-
NC	Not connected	V7	-	-	-	-	-	-
NC	Not connected	V8	-	-	-	-	-	-
NC	Not connected	V9	-	-	-	-	-	-
NC	Not connected	V10	-	-	-	-	-	-
NC	Not connected	V11	-	-	-	-	-	-
NC	Not connected	V12	-	-	-	-	-	-
NC	Not connected	V13	-	-	-	-	-	-
PH10	Headless: SPI2_MOSI HMI: LTDC_R2	V14	GPIO	I/O	PH10	C11	-	-
PB10	Headless: SPI2_CLK HMI: LTDC_R3	V15	GPIO	I/O	PB10	G10	-	-
PB5	Headless: SPI2_MISO HMI: LTDC_B6	V16	GPIO	I/O	PB5	F9	-	-
PB13	Headless: SPI2_CS HMI: FDCAN2_TX	V17	GPIO	I/O	PB13	B10	-	-
PF3	Headless: SPI3_NSS HMI: I2C5_SDA	V18	GPIO	I/O	PF3	B9	-	-
PD12	I2C1_SCL	V19	GPIO	I/O	PD12	D7	-	-
GND	GND	V20	PWR	-	-	-	-	MBC
PB6	ETH2_MDIO	V21	GPIO	I/O	PB6	G3	-	-
PG13	ETH1_TXD0	W1	GPIO	I/O	PG13	R9	-	-
GND	GND	W2	PWR	-	-	-	-	MBC
PI4	BOOT0	W3	BOOT	Input	PI4	P11	-	MBC
PI5	BOOT1	W4	BOOT	Input	PI5	N11	-	MBC
PI6	BOOT2	W5	BOOT	Input	PI6	M11	-	MBC
NC	Not connected	W6	-	-	-	-	-	-
NC	Not connected	W7	-	-	-	-	-	-

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
NRST[23]	NRST	W8	RST	I/O	NRST	K10	Connected to PMIC RST_N and eMMC NRESET. Also, 100nF to GND are included on the SOM.	Add 10nF to GND
NC	Not connected	W9	-	-	-	-	-	-
NC	Not connected	W10	-	-	-	-	-	-
NC	Not connected	W11	-	-	-	-	-	-
VRTC[24]	RTC: VRTC	W12	PWR	Input	-	-	-	-[25]
PH13	Headless: SPI3_SCK HMI: LTDC_G2	W13	GPIO	I/O	PH13	E9	-	-
PH9	Headless: PH9 HMI: LTDC_DE	W14	GPIO	I/O	PH9	D9	-	-
PA1	USART2_RTS	W15	GPIO	I/O	PA1	K8	-	-
PF11	USART2_TX	W16	GPIO	I/O	PF11	L8	-	-
PD5	RAM-Coding_0 HMI: RAM-Coding_0 and LTDC_B0	W17	GPIO	I/O	PD5	B4	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.	-
PD9	RAM-Coding_1 HMI: RAM-Coding_1 and LTDC_CLK	W18	GPIO	I/O	PD9	B5	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.	-
PE8	I2C1_SDA	W19	GPIO	I/O	PE8	F8	-	-
GND	GND	W20	PWR	-	-	-	-	MBC
VBAT	VBAT	W21	PWR	Input	PH13	J5	-	VCC_IO[26]
PG12	ETH1_INTB	Y1	GPIO	I/O	PG12	L6	-	-
GND	GND	Y2	PWR	-	-	-	-	MBC
GND	GND	Y3	PWR	-	-	-	-	MBC
GND	GND	Y4	PWR	-	-	-	-	MBC
GND	GND	Y5	PWR	-	-	-	-	MBC
GND	GND	Y6	PWR	-	-	-	-	MBC
GND	GND	Y7	PWR	-	-	-	-	MBC
GND	GND	Y8	PWR	-	-	-	-	MBC
GND	GND	Y9	PWR	-	-	-	-	MBC
GND	GND	Y10	PWR	-	-	-	-	MBC
GND	GND	Y11	PWR	-	-	-	-	MBC
GND	GND	Y12	PWR	-	-	-	-	MBC
GND	GND	Y13	PWR	-	-	-	-	MBC
GND	GND	Y14	PWR	-	-	-	-	MBC
GND	GND	Y15	PWR	-	-	-	-	MBC
GND	GND	Y16	PWR	-	-	-	-	MBC

[23] A permanent pull-up resistor of ~40k is included in the CPU and an additional ~80k pull-up in the PMIC.
[24] This pin is connected to the RTC RV-3032-C7 Pin 1 (Backup supply voltage). For more information see MicroCrystal datasheet.
[25] See 12.1.2 VRTC.
[26] Must be connected to VCC_IO, if no buffer voltage is connected.

DHCOR pad name	DHCOR default function[1]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes	Pin not used
GND	GND	Y17	PWR	-	-	-	-	MBC
GND	GND	Y18	PWR	-	-	-	-	MBC
GND	GND	Y19	PWR	-	-	-	-	MBC
GND	GND	Y20	PWR	-	-	-	-	MBC
VCC_IO[27]	PMIC: 1V8 or 3V3	Y21	PWR	Output	-	-	-	-
PA11	#ETH1_RST	AA1	GPIO	I/O	PA11	N5	-	-
NC	Not connected	AA2	-	-	-	-	-	-
NC	Not connected	AA3	-	-	-	-	-	-
NC	Not connected	AA4	-	-	-	-	-	-
NC	Not connected	AA5	-	-	-	-	-	-
NC	Not connected	AA6	-	-	-	-	-	-
NC	Not connected	AA7	-	-	-	-	-	-
NC	Not connected	AA8	-	-	-	-	-	-
NC	Not connected	AA9	-	-	-	-	-	-
NC	Not connected	AA10	-	-	-	-	-	-
NC	Not connected	AA11	-	-	-	-	-	-
PB8	I2C3_SCL	AA12	GPIO	I/O	PB8	G4	1.5k PU to VCC_IO and con. to PMIC, EEPRO and RTC.	-
GND	GND	AA13	PWR	-	-	-	-	MBC
PH14	I2C3_SDA	AA14	GPIO	I/O	PH14	B6	1.5k PU to VCC_IO and con. to PMIC, EEPRO and RTC.	-
NC	Not connected	AA15	-	-	-	-	-	-
PB14	SDMMC2_D0	AA16	GPIO	I/O	PB14	A12	Only available without eMMC.	-
PB15	SDMMC2_D1	AA17	GPIO	I/O	PB15	D11	Only available without eMMC.	-
PB3	SDMMC2_D2	AA18	GPIO	I/O	PB3	B11	Only available without eMMC.	-
PB4	SDMMC2_D3	AA19	GPIO	I/O	PB4	E11	Only available without eMMC.	-
PE3	SDMMC2_CK	AA20	GPIO	I/O	PE3	PB12	Only available without eMMC.	-
PG6	SDMMC2_CMD	AA21	GPIO	I/O	PG6	H10	Only available without eMMC.	-

Table 3: Pin assignment

5 Protection circuits

The DHCOR STM32MP13 module does **NOT** contain any protection circuits (e.g. ESD protection). These must be provided from the carrier board.

[27] Connected to STPMIC1D Pin 31. BUCK3 output voltage. For more information see STPMIC1D datasheet.

6 Power supply

The DHCOR-STM32MP13-01LG must be powered by a single 5.0 V supply voltage on the VCC_IN_5V pins. All other voltages are directly generated by the STPMIC1D and can also be used on the carrier board for the supply of peripheral components (Ethernet PHY, eMMC, ...). This enables a carrier board design with only one buck regulator for the 5.0 V DHCOR supply voltage.

Note: The power supply must be buffered with at least two 47uF capacitors on the carrier board.

Furthermore, the STPMIC1D provides two power switches to supply the USB sub-system of the carrier board. These outputs are also directly available on the DHCOR pins SW_OUT and VBUS_OTG.

Summary: The single supply voltage of 5.0 V and the integrated power switches for USB can significantly reduce the efforts and costs of the carrier board.

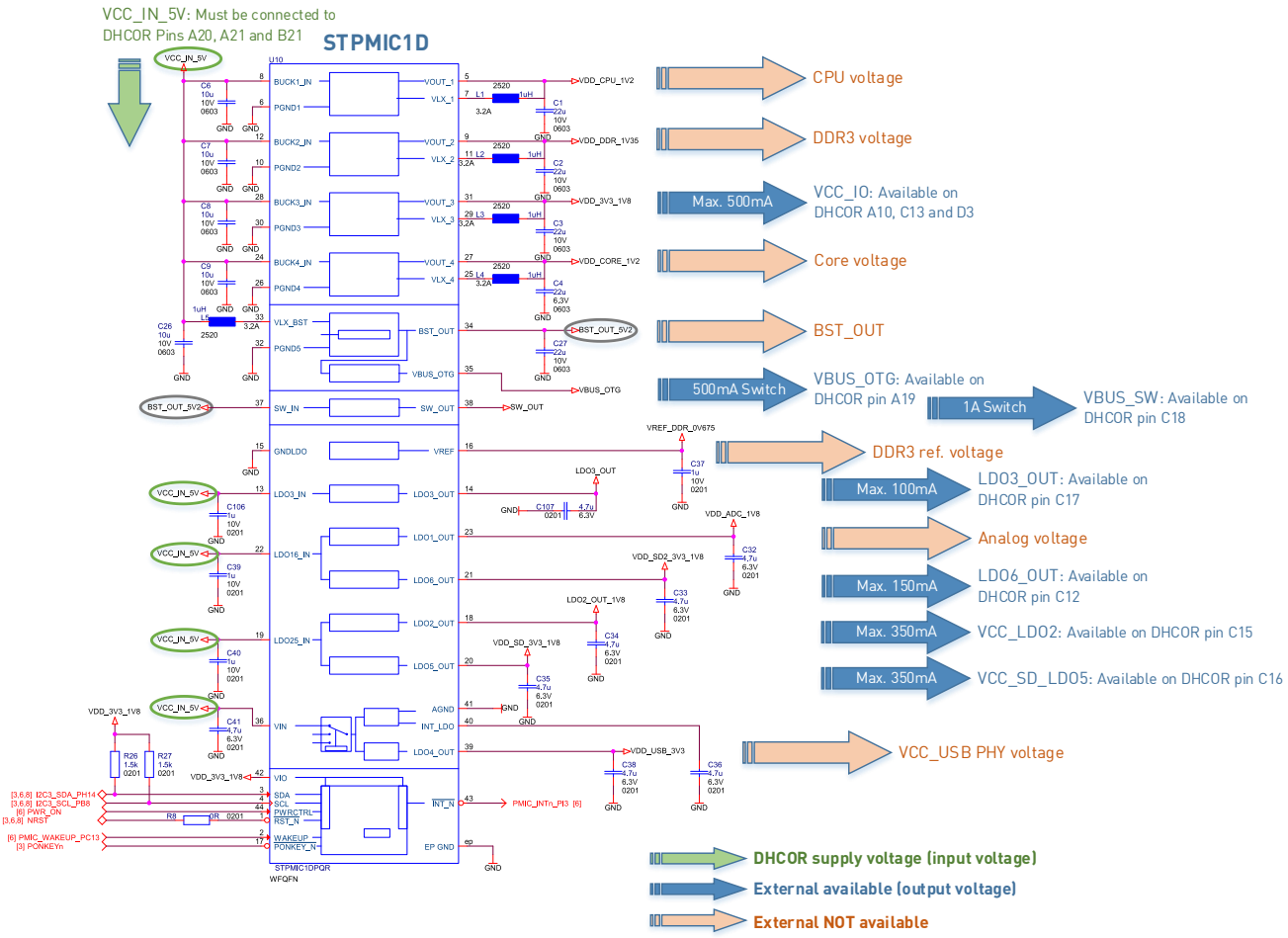


Figure 4: Power supply overview

Notes:

- When designing a carrier board, the EMC performance can be improved by adding filters to the supply voltages of the DHCOR module.

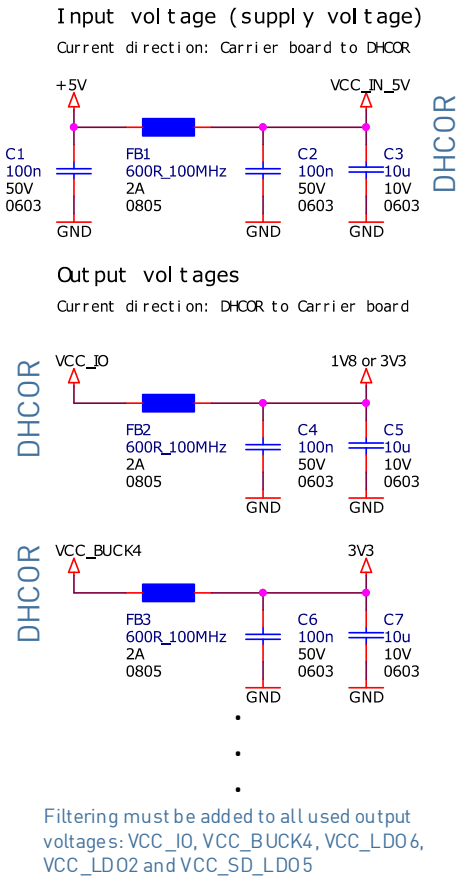


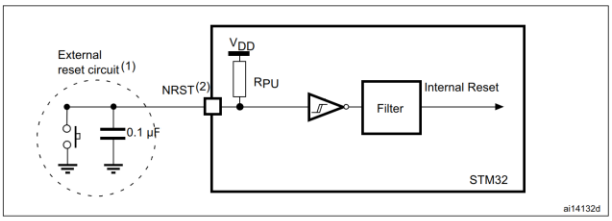
Figure 5: Power supply filtering

Filtering notes:

- Recommended ferrite: Wuerth 742792040 (maximum current of any supply voltage must be checked) or similar
- In case of USB (VBUS_OTG and SW_OUT) no additional filtering is mentioned, because this is added with the standard USB schematic direct to the USB socket.

7 Reset

The reset signal NRST is active low and directly connected to the STM32MP13 NRST pin. VDD is connected to VCC_IO voltage.



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST/NRST_CORE pin can go below the $V_{IL(NRST)}$ max level

Figure 6: Reset

Notes: The 0.1µF capacitor is necessary, even if NRST is not used on the carrier board. It is also recommended to trigger a reset event (from the carrier board) only via an open-drain circuit. Do not connect NRST directly to VCC_IO.

For more precise technical information, we refer you to the ST reset documentation.

8 Boot modes

The STM32MP13 BOOT pins are directly available on the DHCOR pins W3, W4 and W5. No pull-up or pull-down resistors are added to the BOOT pins at the DHCOR module. These parts **MUST** be added external on the carrier board.

The default boot device is the eMMC on the System on Module. Alternatively, there are SOM variants available on which an SPI boot flash is mounted. Depending on the SOM used, the customer must ensure that the boot pin settings on the carrier board are correct, or the OTP settings must be changed.

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB[28]	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins[29]
0	0	1	**Serial NOR-Flash**[30]	Quad SPI boot (located on System-On-Module) [31]
0	1	0	**eMMC**[30]	SDMMC2 = eMMC boot (located on System-On-Module)[31, 32]
0	*1*	*1*	*NAND-Flash*[30]	NAND is not recommended from DH as boot device
1	0	0	Engineering boot (no flash boot) [33]	Used to get debug access without boot from flash memory
1	0	1	**SD card**[30]	SDMMC1: Interface only external available without WiFi/BT[31, 32]
1	1	0	UART and USB[28,30]	Wait incoming connection on: – USART3/6 and UART4/5/7/8 on default pins – USB high-speed device on OTG_HS_DP/DM pins[34]
1	1	1	Serial NAND-Flash[30]	Serial NAND flash on QUADSPI[31]

Table 4: Boot modes

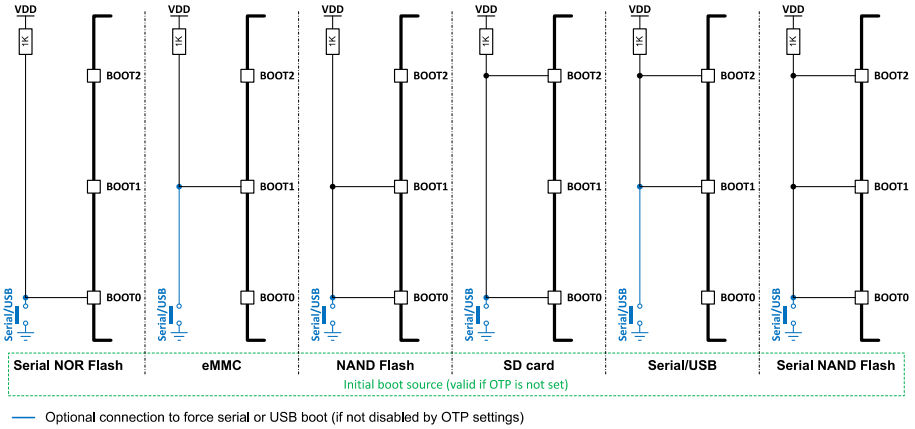


Figure 7: Typical connection schematics of BOOT pins

[28] Can be disabled by OTP settings.
[29] USB requires HSE clock/crystal (see AN5474 for supported frequencies with and without OTP settings).
[30] Boot source can be changed by OTP settings (for example initial boot on SD card, then eMMC with OTP settings).
[31] Default pins can be altered by OTP.
[32] Alternatively, another SDMMC interface than this default can be selected by OTP.
[33] Cortex®-A7 core in infinite loop toggling PA13.
[34] USB requires HSE clock/crystal (see AN5474 for supported frequencies with and without OTP settings).

8.1 SD card boot

Note: SD card boot is only available with a SOM variant without WiFi/BT. Otherwise the SDMMC1 interface is used for WiFi connection.

If the carrier board contains a microSD/SD socket and it is planned to boot form microSD/SD card, it is mandatory to connect the card at the following CPU pins (otherwise SD-Card boot will not work):

- PC12: SDMMC1_CK
- PD2: SDMMC1_CMD
- PC8: SDMMC1_D0

please also have a look at the ST application note AN5474 "**Getting started with STM32MP13x lines hardware development**".

9 eMMC flash memory

As non-volatile data storage, the DHCOR-STM32MP13-01LG module provides an eMMC flash memory to store the bootloader, operating system and application data on it. It is connected to the 8-bit SDMMC2 interface of the STM32MP13 SoC. The size of the eMMC starts from 4 GByte and depends on the ordering configuration.

See also 4.2.1 SDMMC variant overview.

Note: eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly.

Please have a look at: https://en.wikipedia.org/wiki/Flash_memory#Write_endurance

DHCOR pad name	DHCOR default function[35]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PB15	SDMMC2_D1	AA17	GPIO	I/O	PB15	D11	External only available without eMMC.
PB3	SDMMC2_D2	AA18	GPIO	I/O	PB3	B11	External only available without eMMC.
PB4	SDMMC2_D3	AA19	GPIO	I/O	PB4	E11	External only available without eMMC.
PE3	SDMMC2_CK	AA20	GPIO	I/O	PE3	PB12	External only available without eMMC.
PG6	SDMMC2_CMD	AA21	GPIO	I/O	PG6	H10	External only available without eMMC.
-	SDMMC2_D4	-	GPIO	I/O	PF0	A11	External not available.
-	SDMMC2_D5	-	GPIO	I/O	PB9	C10	External not available.
-	SDMMC2_D6	-	GPIO	I/O	PC6	A10	External not available.
-	SDMMC2_D7	-	GPIO	I/O	PC7	A9	External not available.

Table 5: eMMC

[35] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".

10 Quad SPI NOR-Flash

The onboard Quad SPI NOR-Flash is connected to the QuadSPI interface bank1 of the STM32MP13. The used pins are also available on the DHCOR pins. It is possible to order the DHCOR module without onboard Quad SPI NOR-Flash as well. In that case the QuadSPI interface can be used on the carrier board without any limitations. In case the onboard Flash is mounted, it is recommended to left the pins open at the carrier board design, to ensure, that the CPU has full access to the Flash.

DHCOR pad name	DHCOR default function[35]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PB2	QUADSPI_BK1_NCS	J18	GPIO	I/O	PB2	K3	External only available without SPI flash.
PF10	QUADSPI_CLK	J19	GPIO	I/O	PF10	K2	External only available without SPI flash.
PF8	QUADSPI_BK1_IO0	K19	GPIO	I/O	PF8	H3	External only available without SPI flash.
PF9	QUADSPI_BK1_IO1	H19	GPIO	I/O	PF9	H9	External only available without SPI flash.
PD11	QUADSPI_BK1_IO2	L19	GPIO	I/O	PD11	G1	External only available without SPI flash.
PH7	QUADSPI_BK1_IO3	G19	GPIO	I/O	PH7	L3	External only available without SPI flash.

Table 6: Quad SPI NOR-Flash signals

11 EEPROM

The DHCOR STM32MP13 comes with additional 256 kbit onboard EEPROM M24256E from ST. It is connected to the STM32MP13 I2C3 port. Please also have a look at chapter 14 On-Module I2C™

The EEPROM also provides an additional 64 byte identification page area. This area is used by DH electronics to store manufacturer specific information and cannot be used freely. But the normal EEPROM area can be used by the customer without any restrictions.

12 RTC

In addition to the RTC integrated in the STM32MP13, the DHCOR STM32MP13 is available with the optional onboard temperature compensated RTC RV-3032-C7 from Micro Crystal. The RTC is connected to the STM32MP13 I2C3 port. Please also have a look at chapter 14 On-Module I2C™

The additional RTC can be supplied during time keeping mode via a goldcap or a coin cell battery. Therefore, the supply voltage can be applied through the VRTC connection. Please have also a look at 12.1.2 VRTC.

Features:

- Factory calibrated temperature compensation
- Very high Time Accuracy (best in class).
  - ±1.5 ppm 0 to +50°C
  - ±3.0 ppm -40 to +85°C
- Low power consumption: 160 nA @ 3 V.
- Wide operating voltage range: 1.3 V to 5.5 V.
- Aging compensation with OFFSET value
- Counters for hundredths of seconds, seconds, minutes, hours, date, month, year and weekday

Note: The low active INT pin of the RTC is connected to the PI0 port of the STM32MP13.

12.1 VBAT and VRTC: Backup voltage buffering

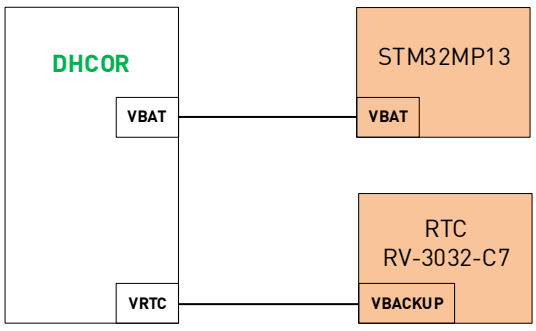


Figure 8: STM32MP13 and RTC VBAT supply

12.1.1 VBAT

The STM32MP13 real-time clock (RTC) and backup registers can be supplied with the VBAT voltage when the main VCC_IO supply is powered off. This internal supply with automatic switch between VBAT and VCC_IO (VDD) is named VSW domain and is also used to supply PC13, PC14, PC15, PI0, PI1, PI2, PI3 pads. When VCC_IO is

above VBAT, a small charging current could be enabled on VBAT for an external backup voltage device (e.g. supercapacitor). For details, please have a look at the ST documentation.

If no external battery is used in the application, it is required to connect VBAT externally to VCC_IO.

12.1.2 VRTC

When ordering the DHCOR STM32MP13 with the option [-RTC], VRTC is connected to the RV-3032-C7 to apply the needed backup voltage from carrier board.

If backup buffering of the additional RTC is not needed, the VRTC pin can be left open. In that case, the RTC is only supplied via VCC_IO and the RTC loses time and date information when the power is switched off.

Please refer to the technical documentation for details: https://www.microcrystal.com/en/products/real-time-clock-rtc-modules/rv-3032-c7/

13 ADC / DAC reference voltage

The PMIC LDO1 (1.8 V by default) is connected as external reference voltage, to the V_{REF+} pin of the STM32MP13 CPU. If it is necessary to use the internal CPU reference voltage or if an external reference voltage must be applied, please contact DH electronics for a special variant of DHCOR-STM32MP13-01LG.

14 On-Module I2C™

By default, the following STM32MP13 pins are used as I2C™ interface on the System on Module.

DHCOR pad name	DHCOR default function[36]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PB8	I2C3_SCL	AA12	GPIO	I/O	PB8	G4	1.5k PU to VCC_IO and con. to PMIC, EEPRO and RTC.
PH14	I2C3_SDA	AA14	GPIO	I/O	PH14	B6	1.5k PU to VCC_IO and con. to PMIC, EEPRO and RTC.

Table 7: On-Module I2C™ interface signals

Only I2C3 is fixed to the I2C™ functionality, because PMIC STPMIC1D, EEPROM and RTC are connected to this interface. Therefore, the pull-up resistors (1k5) to VCC_IO are located at the DHCOR module.

Device		Address (7bit)
PMIC	ST STPMIC1DPQR	0x33
EEPROM	ST M24256E	0x50
RTC	MicroCrystal RV-3032-C7	0x51

Table 8: I2C3 connected devices

[36] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".

15 Wi-Fi® / Bluetooth

The DHCOR STM32MP13 module is available with the optional onboard Wi-Fi® and Bluetooth module Type 1YN from muRata. Wi-Fi® is connected to the 4-bit SDMMC1 interface of the STM32MP13 SoC and Bluetooth® to UART7.

The muRata 1YN uses the Infineon CYW43439 chipset and offers single band 2.4GHz Wi-Fi® and Bluetooth® 5.2 support. Next to this, the module is FCC/IC and MIC (Japan) "Reference" certified and also the ETSI report is available:

15.1 Radio Certification

USA/Canada

- FCC ID: VPYLB1DX
- IC: 772C-LB1DX

Europe

- EN300328 v2.1.1 conducted test report is prepared.

Japan

- Japanese type certification is prepared: R001- P00840

15.2 Bluetooth® Qualification

- QDID: 140301

15.3 Features

Wi-Fi®:

- Wi-Fi® 802.11 b/g/n
- Data rate on Wi-fi® PHY up to 65Mbps
- Single band (2.4 GHz) support
- Network topology: SoftAP and STA dual mode

Bluetooth®:

- Bluetooth® 5.2 BR/EDR/LE
- Data rate on Bluetooth® PHY up to 3Mbps

15.4 32kHz reference clock

The DHCOR Pin C5 LPO_IN_32kHz is connected to the WiFi/BT module 1YN Pin 37. This pin must be connected to an external 32kHz oscillator, if the WiFi/BT module 1YN is mounted on the System on Module. For more information see muRata 1YN datasheet.

15.5 Antenna and connector

On the DHCOR STM32MP13 a standard U.FL. connector from TE 1909763-1 is used. U.FL. is compatible with the IPEX MHF1 connector specification.

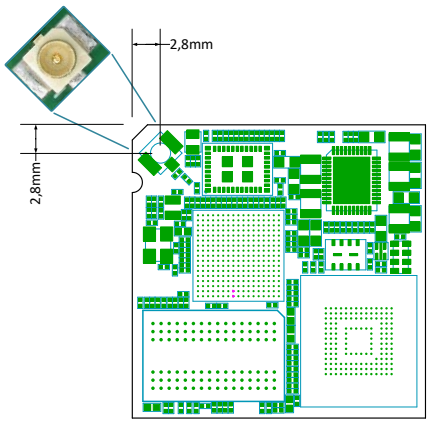


Figure 9: Wi-Fi/BT U.FL. connector

Murata describes the following gain requirements for an external antenna: *The use of an antenna with gain less than 1.4 dBi.*

Therefore, DH recommends the following antenna as a possible external antenna for the DHCOR STM32MP13:

Unictron AA258 - H2B1PC1A1C095L

Figure 10: Unictron AA258

Characteristics:

- Dipole PCB antenna 2.4GHz ~ 2.5GHz with peak gain 2.4GHz @ 0.9dBi.
- 100mm long cable and IPEX MHF I connector.
- -10°C to +85°C (With double-sided tape) and -40°C to +85°C (Without double-sided tape).
- Humidity 10% to 95% RH.

16 Ethernet connection

16.1 1Gbit Ethernet (Headless configuration)

The DHCOR STM32MP13 Development Board (see link tbd...) reference design implements dual 1GBit Ethernet connection.

DHCOR pad name	DH electronics default function[37]	RGMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
PA7	Headless: ETH1_RXCTL HMI: ETH1_CRS_DV	ETH1_RXCTL	E1	GPIO	I/O	PA7	R6
PD7	Headless: ETH1_RXC HMI: PD7	ETH1_RXC	D1	GPIO	I/O	PD7	R3
PC4	ETH1_RXD0	ETH1_RXD0	F1	GPIO	I/O	PC4	K9
PC5	ETH1_RXD1	ETH1_RXD1	G1	GPIO	I/O	PC5	P8
PB0	Headless: ETH1_RXD2 HMI: PB0	ETH1_RXD2	H1	GPIO	I/O	PB0	M8
PB1	Headless: ETH1_RXD3 HMI: PB1	ETH1_RXD3	J1	GPIO	I/O	PB1	N8
PB11	Headless: ETH1_TXCTL HMI: ETH1_TX_EN	ETH1_TXCTL	P1	GPIO	I/O	PB11	M6
PC1	Headless: ETH1_TXC HMI: PC1	ETH1_TXC	R1	GPIO	I/O	PC1	R7
PG13	ETH1_TXD0	ETH1_TXD0	W1	GPIO	I/O	PG13	R9
PG14	ETH1_TXD1	ETH1_TXD1	V1	GPIO	I/O	PG14	T8
PC2	Headless: ETH1_TXD2 HMI: PC2	ETH1_TXD2	U1	GPIO	I/O	PC2	U8
PE5	Headless: ETH1_TXD3 HMI: PE5	ETH1_TXD3	T1	GPIO	I/O	PE5	L9
PG2	ETH1_MDC	ETH1_MDC	C1	GPIO	I/O	PG2	U3
PA2	ETH1_MDIO	ETH1_MDIO	B1	GPIO	I/O	PA2	R5
PG12	ETH1_INTB	ETH1_INTB	Y1	GPIO	I/O	PG12	L6
PA11	#ETH1_RST	#ETH1_RST	AA1	GPIO	I/O	PA11	N5
PA12	Headless: ETH2_RXCTL HMI: ETH2_CRS_DV	ETH2_RXCTL	R21	GPIO	I/O	PA12	F2
PH11	Headless: ETH2_RXC HMI: SPI2_NSS	ETH2_RXC	T21	GPIO	I/O	PH11	H7
PF4	ETH2_RXD0	ETH2_RXD0	P21	GPIO	I/O	PF4	P3
PE2	ETH2_RXD1	ETH2_RXD1	N21	GPIO	I/O	PE2	T1
PH6	Headless: ETH2_RXD2 HMI: SPI2_SCK	ETH2_RXD2	M21	GPIO	I/O	PH6	J6
PA8	Headless: ETH2_RXD3 HMI: SPI2_MOSI	ETH2_RXD3	L21	GPIO	I/O	PA8	J8
PF6	Headless: ETH2_TXCTL HMI: ETH2_TX_EN	ETH2_TXCTL	K21	GPIO	I/O	PF6	L1

[37] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".

DHCOR pad name	DH electronics default function[37]	RGMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
PG3	Headless: ETH2_TXC HMI: FDCAN2_RX	ETH2_TXC	J21	GPIO	I/O	PG3	U2
PF7	ETH2_TXD0	ETH2_TXD0	E21	GPIO	I/O	PF7	J7
PG11	ETH2_TXD1	ETH2_TXD1	F21	GPIO	I/O	PG11	R1
PG1	Headless: ETH2_TXD2 HMI: SPI2_MISO	ETH2_TXD2	G21	GPIO	I/O	PG1	P4
PE6	Headless: ETH2_TXD3 HMI: LTDC_G3	ETH2_TXD3	H21	GPIO	I/O	PE6	R2
PG5	ETH2_MDC	ETH2_MDC	U21	GPIO	I/O	PG5	H1
PB6	ETH2_MDIO	ETH2_MDIO	V21	GPIO	I/O	PB6	G3
PG15	ETH2_INTB	ETH2_INTB	D21	GPIO	I/O	PG15	G8
PG8	#ETH2_RST	#ETH2_RST	C21	GPIO	I/O	PG8	J3

Table 9: Ethernet 1Gbit RGMII signals

16.2 100Mbit Ethernet (Headless configuration)

This chapter shows how to connect two 100MBit PHY's to the DHCOR-STM32MP13-01LG with headless default configuration:

DHCOR pad name	DH electronics default function[38]	RMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
PA7	Headless: ETH1_RXCTL HMI: ETH1_CRS_DV	ETH1_CRS_DV	E1	GPIO	I/O	PA7	R6
PC4	ETH1_RXD0	ETH1_RXD0	F1	GPIO	I/O	PC4	K9
PC5	ETH1_RXD1	ETH1_RXD1	G1	GPIO	I/O	PC5	P8
PB11	Headless: ETH1_TXCTL HMI: ETH1_TX_EN	ETH1_TX_EN	P1	GPIO	I/O	PB11	M6
PG13	ETH1_TXD0	ETH1_TXD0	W1	GPIO	I/O	PG13	R9
PG14	ETH1_TXD1	ETH1_TXD1	V1	GPIO	I/O	PG14	T8
PG2	ETH1_MDC	ETH1_MDC	C1	GPIO	I/O	PG2	U3
PA2	ETH1_MDIO	ETH1_MDIO	B1	GPIO	I/O	PA2	R5
PG12	ETH1_INTB	ETH1_INTB	Y1	GPIO	I/O	PG12	L6
PA11	#ETH1_RST	#ETH1_RST	AA1	GPIO	I/O	PA11	N5
PD7	Headless: ETH1_RXC HMI: PD7	*not required → free to use*	D1	GPIO	I/O	PD7	R3
PB0	Headless: ETH1_RXD2 HMI: PB0	*not required → free to use*	H1	GPIO	I/O	PB0	M8
PB1	Headless: ETH1_RXD3 HMI: PB1	*not required → free to use*	J1	GPIO	I/O	PB1	N8
PC1	Headless: ETH1_TXC HMI: PC1	*not required → free to use*	R1	GPIO	I/O	PC1	R7
PC2	Headless: ETH1_TXD2 HMI: PC2	*not required → free to use*	U1	GPIO	I/O	PC2	U8
PE5	Headless: ETH1_TXD3	*not required → free to use*	T1	GPIO	I/O	PE5	L9

[38] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".

DHCOR pad name	DH electronics default function[38]	RMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
	HMI: PE5						
PA12	Headless: ETH2_RXCTL HMI: ETH2_CRS_DV	ETH2_CRS_DV	R21	GPIO	I/O	PA12	F2
PF4	ETH2_RXD0	ETH2_RXD0	P21	GPIO	I/O	PF4	P3
PE2	ETH2_RXD1	ETH2_RXD1	N21	GPIO	I/O	PE2	T1
PF6	Headless: ETH2_TXCTL HMI: ETH2_TX_EN	ETH2_CRS_DV	K21	GPIO	I/O	PF6	L1
PF7	ETH2_TXD0	ETH2_TXD0	E21	GPIO	I/O	PF7	J7
PG11	ETH2_TXD1	ETH2_TXD1	F21	GPIO	I/O	PG11	R1
PG5	ETH2_MDC	ETH2_MDC	U21	GPIO	I/O	PG5	H1
PB6	ETH2_MDIO	ETH2_MDIO	V21	GPIO	I/O	PB6	G3
PG15	ETH2_INTB	ETH2_INTB	D21	GPIO	I/O	PG15	G8
PG8	#ETH2_RST	#ETH2_RST	C21	GPIO	I/O	PG8	J3
PH11	Headless: ETH2_RXC HMI: SPI2_NSS	*not required → free to use*	T21	GPIO	I/O	PH11	H7
PH6	Headless: ETH2_RXD2 HMI: SPI2_SCK	*not required → free to use*	M21	GPIO	I/O	PH6	J6
PA8	Headless: ETH2_RXD3 HMI: SPI2_MOSI	*not required → free to use*	L21	GPIO	I/O	PA8	J8
PG3	Headless: ETH2_TXC HMI: FDCAN2_RX	*not required → free to use*	J21	GPIO	I/O	PG3	U2
PG1	Headless: ETH2_TXD2 HMI: SPI2_MISO	*not required → free to use*	G21	GPIO	I/O	PG1	P4
PE6	Headless: ETH2_TXD3 HMI: LTDC_G3	*not required → free to use*	H21	GPIO	I/O	PE6	R2

Table 10: Ethernet 100Mbit RMII signals (headless)

16.3 100Mbit Ethernet (HMI configuration)

This chapter shows how to connect two 100MBit PHY's to the DHCOR-STM32MP13-01LG with HMI default configuration:

DHCOR pad name	DH electronics default function[39]	RMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
PA7	Headless: ETH1_RXCTL HMI: ETH1_CRS_DV	ETH1_CRS_DV	E1	GPIO	I/O	PA7	R6
PC4	ETH1_RXD0	ETH1_RXD0	F1	GPIO	I/O	PC4	K9
PC5	ETH1_RXD1	ETH1_RXD1	G1	GPIO	I/O	PC5	P8
PB11	Headless: ETH1_TXCTL HMI: ETH1_TX_EN	ETH1_TX_EN	P1	GPIO	I/O	PB11	M6
PG13	ETH1_TXD0	ETH1_TXD0	W1	GPIO	I/O	PG13	R9
PG14	ETH1_TXD1	ETH1_TXD1	V1	GPIO	I/O	PG14	T8
PG2	ETH1_MDC	ETH1_MDC	C1	GPIO	I/O	PG2	U3
PA2	ETH1_MDIO	ETH1_MDIO	B1	GPIO	I/O	PA2	R5

[39] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".

DHCOR pad name	DH electronics default function[39]	RMII signal	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball
PG12	ETH1_INTB	ETH1_INTB	Y1	GPIO	I/O	PG12	L6
PA11	#ETH1_RST	#ETH1_RST	AA1	GPIO	I/O	PA11	N5
PA12	Headless: ETH2_RXCTL HMI: ETH2_CRS_DV	ETH2_CRS_DV	R21	GPIO	I/O	PA12	F2
PF4	ETH2_RXD0	ETH2_RXD0	P21	GPIO	I/O	PF4	P3
PE2	ETH2_RXD1	ETH2_RXD1	N21	GPIO	I/O	PE2	T1
PF6	Headless: ETH2_TXCTL HMI: ETH2_TX_EN	ETH2_CRS_DV	K21	GPIO	I/O	PF6	L1
PF7	ETH2_TXD0	ETH2_TXD0	E21	GPIO	I/O	PF7	J7
PG11	ETH2_TXD1	ETH2_TXD1	F21	GPIO	I/O	PG11	R1
PG5	ETH2_MDC	ETH2_MDC	U21	GPIO	I/O	PG5	H1
PB6	ETH2_MDIO	ETH2_MDIO	V21	GPIO	I/O	PB6	G3
PG15	ETH2_INTB	ETH2_INTB	D21	GPIO	I/O	PG15	G8
PG8	#ETH2_RST	#ETH2_RST	C21	GPIO	I/O	PG8	J3

Table 11: Ethernet 100Mbit RMII signals (HMI)

17 Display / RGB connection

The STM32MP13 provides a native 24-bit parallel digital RGB (Red, Green, Blue) interface with the following features:

- 2 input layers blended together to compose the display
- Cropping of layers from any input size and location
- Multiple input pixel formats:
  - Predefined ARGB, with 7 formats: ARGB8888, ABGR8888, RGBA8888, BGRA8888, RGB565, BGR565, RGB888packed
  - Flexible ARGB, allowing any width and location for A,R,G,B components
  - Predefined YUV, with 3 formats: YUV422-1L (FourCC: YUYV, Interleaved), YUV420-2L (FourCC: NV12, semi planar), YUV420-3L (FourCC: Yxx, full planar) with some flexibility on the sequence of the component.
- Color look-up table (CLUT) up to 256 colors (256x24 bits) per layer
- Color transparency keying
- Composition with flexible window position and size versus output display
- Blending with flexible layer order and alpha value (per pixel or constant)
- Background underlying color
- Gamma with non-linear configurable table
- Dithering for output with less bits per component (pseudo-random on 2 bits)
- Polarity inversion for HSync, VSync, and DataEnable outputs
- Output as RGB888 24 bpp or YUV422 16 bpp
- Interrupts based on 7 different events
- AXI master interface with long efficient bursts (64 or 128 bytes)

DHCOR pad name	DH electronics default function[36]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PH9	Headless: PH9 HMI: LTDC_DE	W14	GPIO	I/O	PH9	D9	-
PD9	RAM-Coding_1 HMI: RAM-Coding_1 and LTDC_CLK	W18	GPIO	I/O	PD9	B5	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PE1	Headless: PE1 HMI: LTDC_HSYNC	D18	GPIO	I/O	PE1	C3	-
PG4	Headless: PG4 HMI: LTDC_VSYNC	H18	GPIO	I/O	PG4	C9	-
PE11	Headless: SAI1_FS_A HMI: LTDC_R0	F18	GPIO	I/O	PE11	E4	-
PD4	Headless: SPI3_MISO	E18	GPIO	I/O	PD4	A2	-

DHCOR pad name	DH electronics default function[36]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
	HMI: LTDC_R1						
PH10	Headless: SPI2_MOSI HMI: LTDC_R2	V14	GPIO	I/O	PH10	C11	-
PB10	Headless: SPI2_CLK HMI: LTDC_R3	V15	GPIO	I/O	PB10	G10	-
PD14	Headless: TIM4_CH3 HMI: LTDC_R4	N18	GPIO	I/O	PD14	F7	-
PE7	Headless: PE7 HMI: LTDC_R5	N19	GPIO	I/O	PE7	C4	-
PE13	Headless: I2C5_SDA HMI: LTDC_R6	C19	GPIO	I/O	PE13	C1	-
PE9	Headless: SPI2_RST HMI: LTDC_R7	M19	GPIO	I/O	PE9	A3	-
PF5	Headless: PF5 HMI: LTDC_G0	D16	GPIO	I/O	PF5	D1	-
PF1	Headless: SPI3_MOSI HMI: LTDC_G1	R18	GPIO	I/O	PF1	A8	-
PH13	Headless: SPI3_SCK HMI: LTDC_G2	W13	GPIO	I/O	PH13	E9	-
PE6	Headless: ETH2_TXD3 HMI: LTDC_G3	H21	GPIO	I/O	PE6	R2	-
PD13	Headless: Mainboard-HW-CODING_1 and PD13 HMI: Mainboard-HW-CODING_1 and LTDC_G4	D14	GPIO	I/O	PD13	N1	-
PG0	Headless: FDCAN2_TX HMI: LTDC_G5	F19	GPIO	I/O	PG0	A4	-
PE12	Headless: SPI2_PIRQ HMI: LTDC_G6	A17	GPIO	I/O	PE12	B1	-
PA15	Headless: Mainboard-HW-CODING_2 and PA15 HMI: Mainboard-HW-CODING_2 and LTDC_G7	G18	GPIO	I/O	PA15	E7	-
PD5	RAM-Coding_0 HMI: RAM-Coding_0 and LTDC_B0	W17	GPIO	I/O	PD5	B4	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PE0	Headless: FDCAN2_RX HMI: LTDC_B1	E19	GPIO	I/O	PE0	B3	-
PD10	Headless: PD10 HMI: LTDC_B2	D17	GPIO	I/O	PD10	D3	-
PF2	Headless: #USB_PWR_FLT HMI: LTDC_B3	U19	GPIO	I/O	PF2	B7	-
PH3	Headless: Mainboard-HW-CODING_0 and PH3 HMI: Mainboard-HW-CODING_0 and LTDC_B4	D15	GPIO	I/O	PH3	T2	-
PD15	Headless: USART2_RX	P19	GPIO	I/O	PD15	A5	-

DHCOR pad name	DH electronics default function[36]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
	HMI: LTDC_B5						
PB5	Headless: SPI2_MISO HMI: LTDC_B6	V16	GPIO	I/O	PB5	F9	-
PE15	Headless: USART2_CTS HMI: LTDC_B7	T19	GPIO	I/O	PE15	A6	-

Table 12: RGB display signals

18 Hardware and DDR3 coding

The following pins are used by DH electronics for hardware and DDR3 size coding:

DHCOR pad name	DH electronics default function[36]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PA13	HW-CODING_0	J4	GPIO	I/O	PA13	K7	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PI1	HW-CODING_1	K4	GPIO	I/O	PI1	N4	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PD5	RAM-Coding_0 HMI: RAM-Coding_0 and LTDC_B0	W17	GPIO	I/O	PD5	B4	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PD9	RAM-Coding_1 HMI: RAM-Coding_1 and LTDC_CLK	W18	GPIO	I/O	PD9	B5	Used for hardware coding on the SOM. 10k PU or PD connected on the SOM.
PH3	Headless: Mainboad-HW-CODING_0 and PH3 HMI: Mainboard-HW-CODING_0 and LTDC_B4	D15	GPIO	I/O	PH3	T2	-
PD13	Headless: Mainboard-HW-CODING_1 and PD13 HMI: Mainboard-HW-CODING_1 and LTDC_G4	D14	GPIO	I/O	PD13	N1	-
PA15	Headless: Mainboard-HW-CODING_2 and PA15 HMI: Mainboard-HW-CODING_2 and LTDC_G7	G18	GPIO	I/O	PA15	E7	-

Table 13: Hardware and DDR3 coding pins

Hardware (PCB) version	PI1: HW Code bit 1	PA13: HW Code bit 0
HW100 (version 1)	0	0
HW200 (version 2)	0	1
HW300 (version 3)	1	0
HW400 (version 4)	1	1

Table 14: Hardware coding

DDR3 size	PD9: RAM Code bit 1	PD5: RAM Code bit 0
128 Mbyte (not available)	0	0
256 MByte	0	1
512 MByte	1	0
1024 MByte	1	1

Table 15: DDR3 coding

Note:

- 1 = 10k pull-up at DHCOR module
- 0 = 10k pull-down at DHCOR module

Mainboard-HW (PCB) version	PA15: HW Code bit 2	PD13: HW Code bit 1	PH3: HW Code bit 0
HW100 (version 1)	0	0	0
HW200 (version 2)	0	0	1
HW300 (version 3)	0	1	0
HW400 (version 4)	0	1	1
...			
HW800 (version 8)	1	1	1

Table 16: Mainboard-HW coding

Note:

- 1 = A 10k pull-up should be placed on the mainboard to allow the coding to be used in dedicated customer projects.
- 0 = A 10k pull-down should be placed on the motherboard to allow the coding to be used in dedicated customer projects.

Due to this the bootloader (U-Boot) scans the states of these pins during startup, starts the correct memory initialization and provides information regarding the PCB version in order to handle possible PCB differences correctly. The coding pins can be also used for alternate functions, but the customer must remove the pin scanning from bootloader and ensure the initialization of the DDR3 memory with the correct initialization values.

Important for customer mainboard design:

The same belongs to the mainboard-HW hardware version pins, but these pins should be used in a customer mainboard design to provide the customer mainboard hardware information to the bootloader.

19 JTAG / SWD connection

The standard JTAG and SWD interface is directly available at the following DHCOR pins:

DHCOR pad name	DH electronics default function[40]	DHCOR pad	Ball Type	Input/ Output	CPU ball name	CPU ball	Notes
PH4	DEBUG_JTDI	M3	GPIO	I/O	PH4	T13	-
PF15	DEBUG_JTMS-SWDIO	N4	GPIO	I/O	PF15	L10	-
PF14	DEBUG_JTCK-SWCLK	J3	GPIO	I/O	PF14	U4	-
PH5	DEBUG_JTDO-SWO	R4	GPIO	I/O	PH5	L12	-
DEBUG_JTRST	DEBUG_JTRST	P4	GPIO	Input	NJTRST	R10	-
NRST[41]	NRST	W8	RST	I/O	NRST	K10	Connected to PMIC RST_N and eMMC NRESET. Also, 100nF to GND are included on the SOM.

Table 17: JTAG / SWD pins

To avoid uncontrolled, I/O levels the STM32MP1 series embeds internal pull-up and pull-down resistors on the JTAG pins:

- SYS_JTRST: Internal pull-up
- SYS_JTDI: Internal pull-up
- SYS_JTDO-SWO: Internal pull-up
- SYS_JTMS-SWDIO: Internal pull-up
- SYS_JTCK-SWCLK: Internal pull-down

The next figure shows the connection between the STM32MP1 series and a standard JTAG/SWD connector:

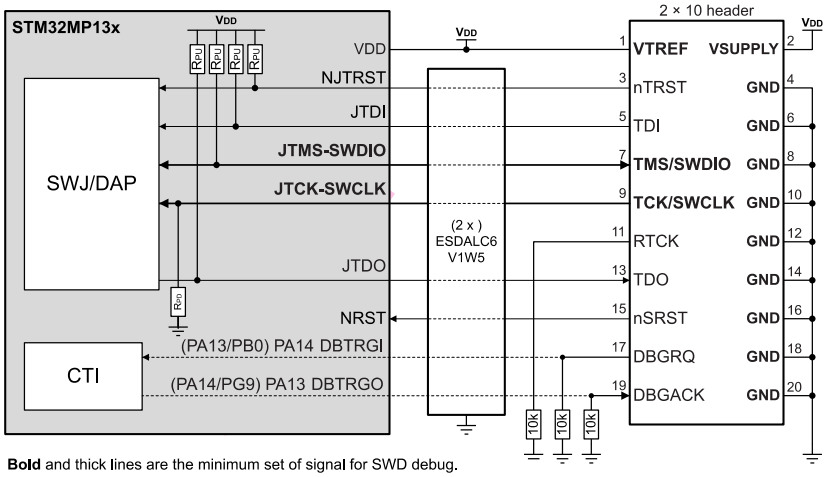


Figure 11: JTAG / SWD Connection

[40] "DHCOR default function" means Development Board configuration (headless) or HMI example configuration from above. If the default configuration differs between both, then the default function is marked with "headless" or "HMI".
[41] A permanent pull-up resistor of ~40k is included in the CPU and an additional ~80k pull-up in the PMIC.

20 UART for bootloader and Linux console

It is strongly recommended to use one UART interface to enable access to the bootloader and linux console on the carrier board. The port can be deactivated during production to avoid illegal access to the series device, but for development and prototyping this port should be accessible.

On the DHCOR STM32MP13 Development Board, the following pins are used for bootloader and linux console:

- PA9: UART4_TX
- PD8: UART4_RX

21 USB boot and flash programming

It is strongly recommended to enable the access to the USB OTG port on the carrier board and the possibility to switch to USB boot mode. Then the standard Linux dfu-util can be used to start up the board or the STM32CubeProgrammer can be used to program any flash device supported on STM32MPU boards:

- microSD™ card
- eMMC
- NOR Flash memory
- NAND Flash memory

STM32CubeProgrammer is the official STMicroelectronics tool for creating partitions into any Flash device available on STM32 platforms. Once created, STM32CubeProgrammer allows populating and updating the partitions with the prebuilt binaries. The connection between the host PC and the board can be done through UART or USB serial links.

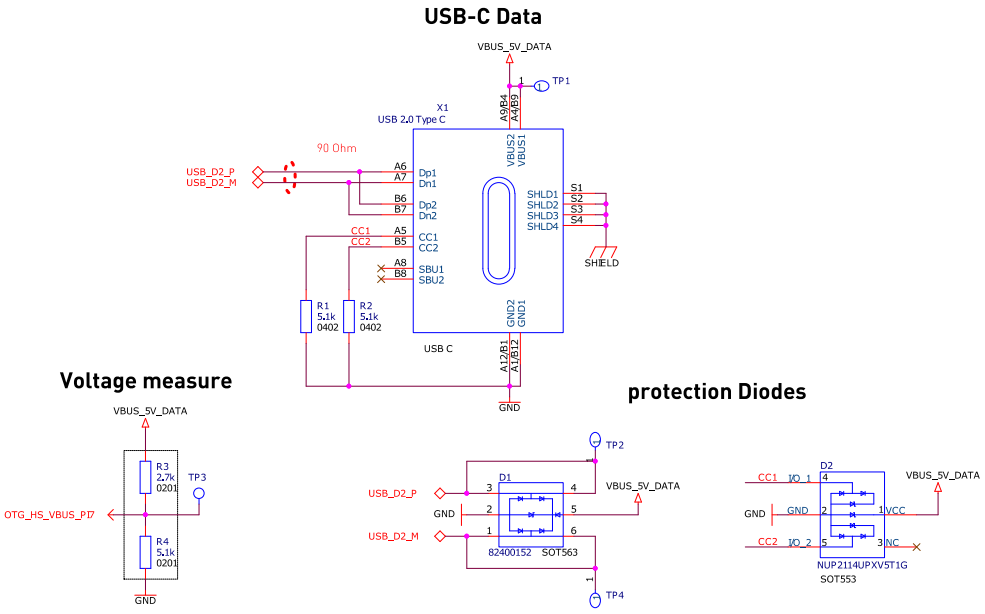


Figure 12: Simple USB Type-C example

Note: If needed, OTG_HS_VBUS and OTG_HS_ID signals are already available on some GPIOs. OTG_HS_VBUS is on PI7 (EXTI7) and OTG_HS_ID is on PA10 (EXTI10).

22 Technical specifications

22.1 Operating conditions – Absolute maximum / operating conditions

Symbol	Description	Input / Output	Min	Typ	Max	Unit
VCC_IN_5V	5V supply voltage	Input	4.2	5.0	5.5	V
$P_{VCC\_IN\_5V}$ [42]	Max. power consumption w/o WiFi/BT	Input	-	Tbd	See 22.2	W
	Max. power consumption with WiFi/BT	Input	-	Tbd	See 22.2	W
$VCC\_IN\_5V_{ripple}$	VCC ripple peak-to-peak	Input	-	30	60	mV
VBAT	STM32MP13 Backup operating voltage	Input	1.2	-	3.6	V
I_{VBAT}	Max. backup current	Input	-	-	90.8	µA
VRTC	RTC backup supply voltage	Input	1.1	-	5.5	V
I_{VRTC}	Max. backup current	Input	-	160	180	nA
VBAT_WIFI	External WiFi power supply	Input	Do not connect this pin. Only usable with customer specific variant.			
VCC_IO	IO voltage	Output	-	3.3	-	V
I_{VCC_IO} [43]	Max. usable VCC_IO output current (with WiFi/BT)	Output	-	-	100	mA
LDO2_OUT	LDO2 voltage	Output	1.7	1.8	3.3	V
I_{LDO2_OUT}	Max. usable LDO2_OUT output current	Output	-	-	350	mA
LDO3_OUT	LDO3 voltage	Output	1.8	1.8	3.3	V
I_{LDO3_OUT}	Max. usable LDO3_OUT output current	Output	-	-	100	mA
LDO5_OUT	LDO5 voltage	Output	1.7	3.3	3.9	V
I_{LDO5_OUT}	Max. usable LDO5_OUT output current	Output	-	-	350	mA
LDO6_OUT	LDO6 voltage	Output	0.9	1.0	3.3	V
I_{LDO6_OUT}	Max. usable LDO6 output current	Output	-	-	150	mA
VBUS_OTG	5V USB OTG power switch	Output	-	5.0	5.2	V
I_{VBUS_OTG}	Max. usable VBUS_OTG output current	Output	-	-	500	mA
SW_OUT	5V USB Host power switch	Output	-	5.0	5.2	V
I_{SW_OUT}	Max. usable SW_OUT output current**Fehler! Textmarke nicht definiert.**	Output	-	-	1000	mA
V_{IL}	I/O input low level voltage for VCC_IO = 3.3V	Input	-	-	0.3xVCC_IO	V
V_{IH}	I/O input high level voltage	Input	0.7xVCC_IO	-	-	V

Table 18: DC operating conditions

Note: The carrier board designer MUST always consider the thermal conditions on the DHCOR module.

22.2 DHCOR max. power consumption

Symbol	Description	Power symbol	Max. power value
VDD_CORE[44]	Digital core supply voltage	$P_{VDD\_CORE\_MAX}$	0.26 W (213 mA @ 1.2 V @ 85°C)
VDD_CPU[44]	ARM-core supply voltage	$P_{VDD\_CPU\_MAX}$	0.27 W (225 mA @ 1.2 V @ 1GHz @ 85°C)
VCC_DDR	DDR3 supply voltage	$P_{VCC\_DDR\_MAX}$	0.34 W (250 mA @ 1.35 V)

[42] Only DHCOR STM32MP13 without any output power consumption.
[43] VCC_IO System on Module current consumption: PMIC = 1mA, SoC = 100mA, EEPROM = 1mA, QuadSPI = 25mA, RTC = 1mA, eMMC = 300mA, WiFi/BT = 370mA → max. 428mA w/o WiFi/BT and 798mA with WiFi/BT
[44] The values based on STM32MP135F core.

Symbol	Description	Power symbol	Max. power value
VCC_IO[43]	IO supply voltage	$P_{VCC\_IO\_WITH\_WIFI/BT\_MAX}$	2.63 W (798 mA @ 3.3 V)
		$P_{VCC\_IO\_W/O\_WIFI/BT\_MAX}$	1.41 W (428 mA @ 3.3 V)
VREF_DDR	DDR3 reference voltage	P_{VREF_DDR}	0.003 W (5 mA @ 0.675 V)
VCCA	Analog operation voltage	P_{VCCA}	Tbd (tbd @ 1.8 V)
VCC_USB	USB supply voltage	P_{VCC_USB}	Tbd (tbd @ 3.3 V)
Maximum DHCOR power consumption			**2.28 W** (w/o WiFi/BT) **3.50 W** (with WiFi/BT) [45]

Table 19: DHCOR max. power consumption

22.3 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
RST#	System Reset input assertion time (active low)	20[46]	-	-	µs
RST#	System Reset output power-cycle (active low)	-	27.8	-	ms

Table 20: Reset Timings

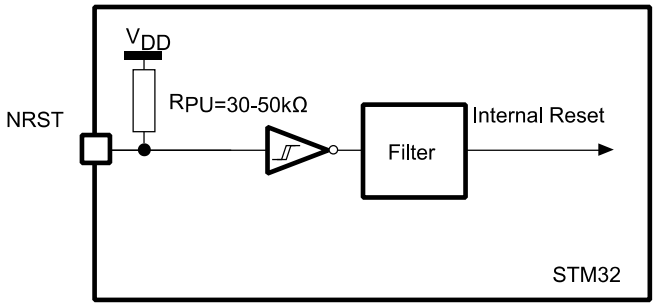


Figure 13: MP1 reset pad (MPU internal circuit)

22.4 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range w/o WiFi/BT[47]	-25		85	°C
T_AMB	Operating temperature range with WiFi/BT	-25		70	°C

Table 21: Temperature range

[45] Please include an adequate buffer in the power supply design.
[46] PMIC RSTnDB time
[47] Negative temperature is limited with standard eMMC. -40°C on request.

23 Mechanical specifications

23.1 Dimensions

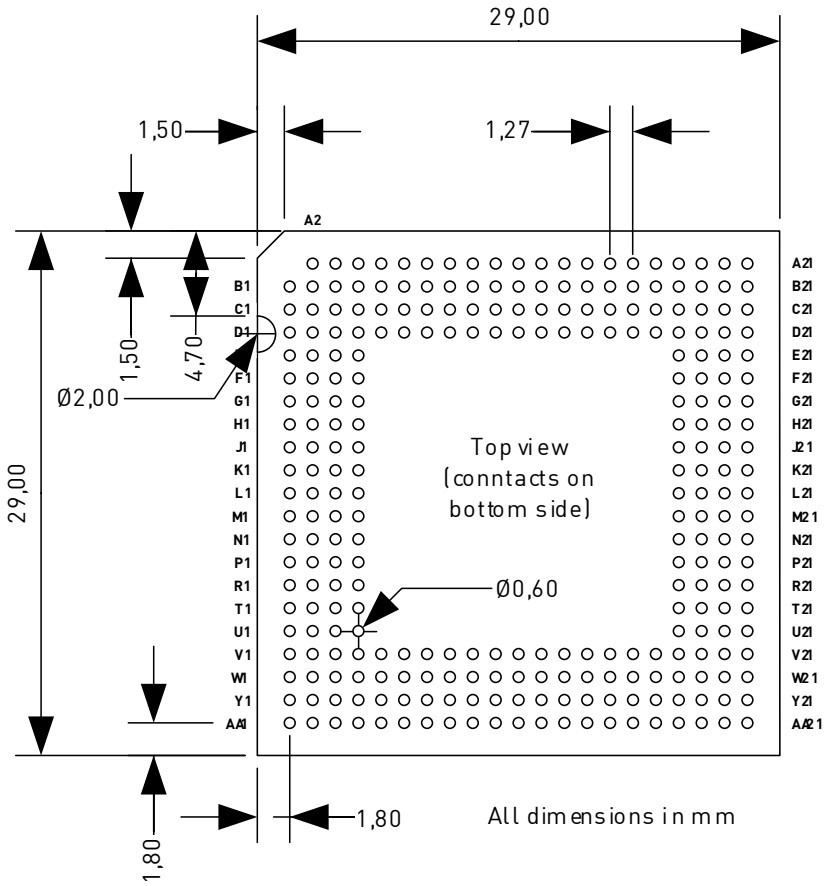


Figure 14: Dimensions of the module

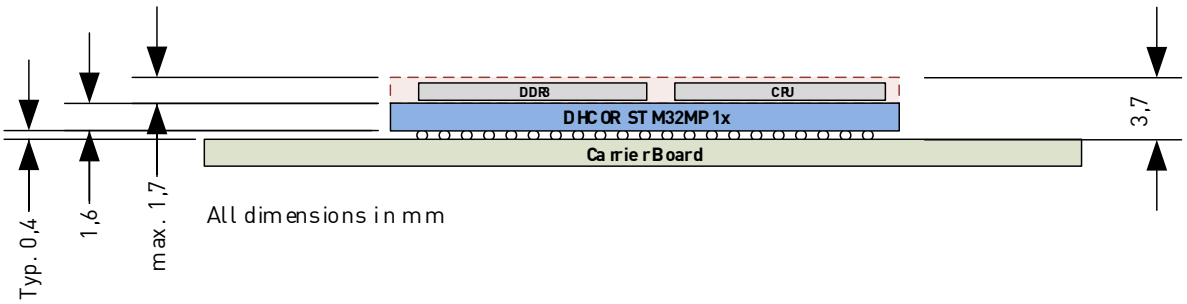


Figure 15: DHCOR height[48]

[48] Max. 3.7mm without U.FL connector counterpart.

23.2 PCB land pattern

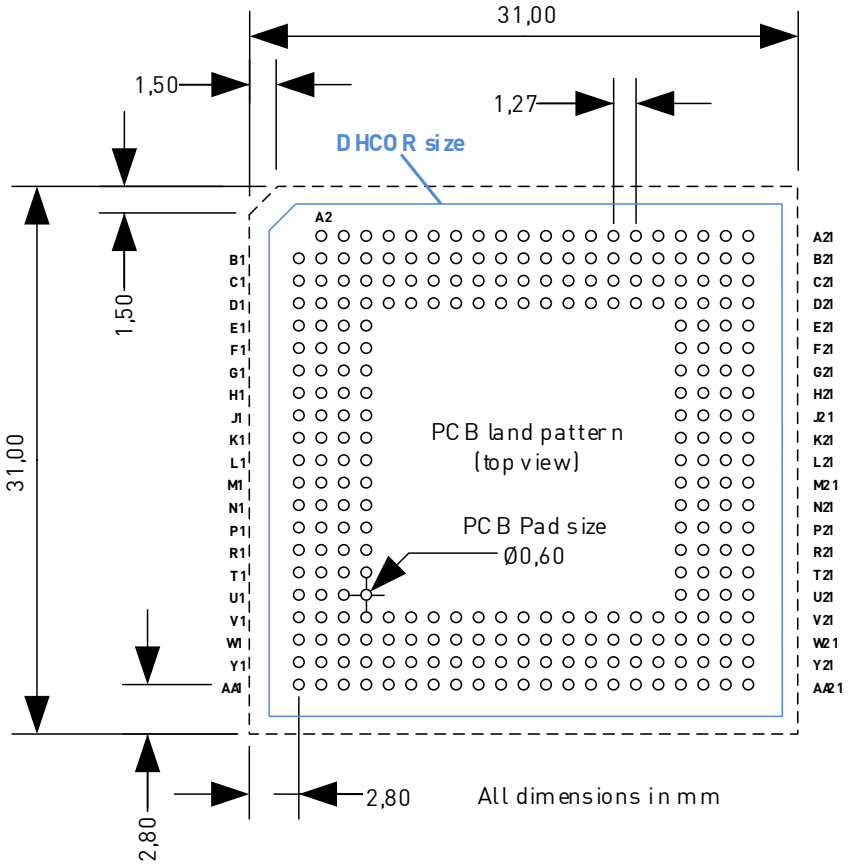


Figure 16: PCB land pattern

24 Assembly instructions

DHCOR-STM32MP13-01LG has been designed for SMT mounting of the module on the carrier board. The DHCOR uses LGA contact pads on the bottom side for the connection to the carrier board. During the production process of the module solder paste is applied to the LGA pads. Therefore, the DHCOR is nearly similar to a BGA. The solder paste on the pads improves the contact quality between module and carrier board, compared with a standard LGA part (without solder paste on the module pads).

24.1 Moisture sensitivity and shelf life

- Calculated shelf life in tape and real packaging: 12 months at < 40 °C and < 90 % relative humidity (RH).
- The DHCOR-STM32MP13-01LG is applicable to MSL3 (based on IPC/JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at < 30 °C and < 60 % RH and the product shall be used within 168 hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 $^{+5}/_{-0}$ °C, 24 hours, 1 time
- The products shall be baked on a heat-resistant tray since the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

24.2 Coplanarity

Coplanarity of the carrier board: < 0.1 mm

24.3 Solder pastes

Solder paste parameters:

- Any lead-free (Pb-free) SAC solder pastes can be used.

Solder paste print parameters:

- Stencil thickness: > 0.1 mm (recommended 0.15 mm)
- Stencil pad diameter: Suggestion 0.55 mm (0.6 mm pad size)

24.4 Reflow Process

Use reflow profiles per IPC/JEDEC J-STD-020D.

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_L)	 150 °C 200 °C 60-120 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60-150 °C
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6°C/second max.
Time 25 °C to peak temperature	8 minutes max.

Table 22: Reflow profil per IPC/JEDEC J-STD-020E

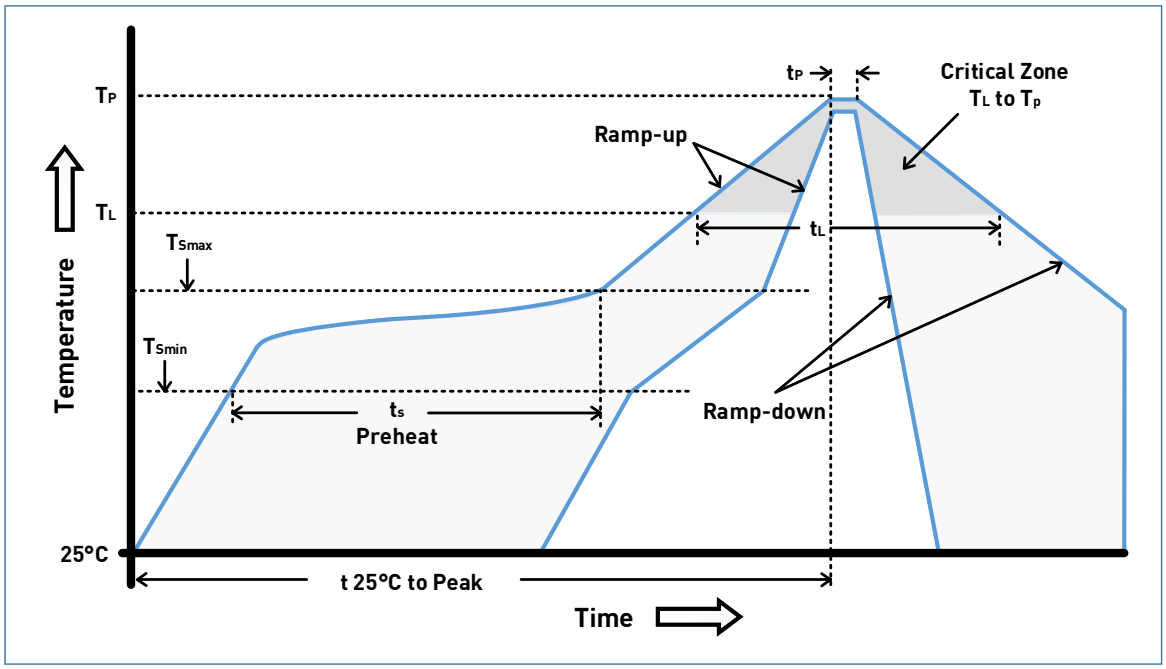


Figure 17: Reflow Classification Profile

The manufacturing of the DHCOR-STM32MP13-01LG requires two reflow cycles. Two reflow cycles are remaining for mounting the module on the carrier board. It is strongly recommended to solder the DHCOR-STM32MP13-01LG module during the last reflow cycle of the carrier board manufacturing process.

25 Tape and reel packaging

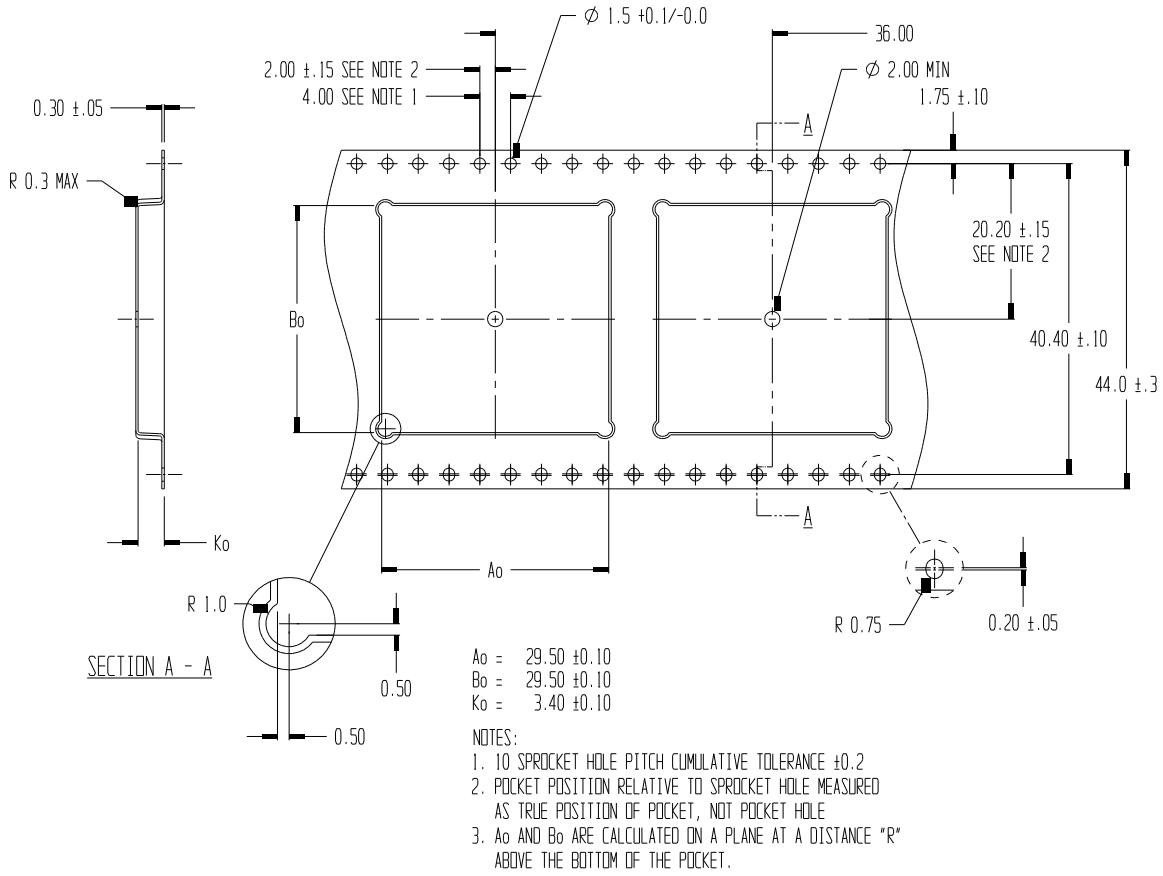


Figure 18: Tape and reel packaging

26 Hardware design checklist

Table 23 is a checklist for all the important design guidelines. Please read each checklist entry carefully to ensure that your carrier board design meets these guidelines.

Number	Checklist / Design notes
1	It is recommended to reuse the DHCOR pin assignment of the reference Designs “headless” or “HMI” as far as possible in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can be taken from these examples, without any BSP porting efforts. Please have a look at chapter 4.4 Pin-Mux example configurations
2	Does the carrier board design provide any connection to the JTAG pins (e.g. mounting option, only for development)? Please have a look at chapter 19 JTAG / SWD connection
3	Are the BOOT pins provided with correct pull-up or pull-down resistors for the preferred boot options? Please have a look at chapter 8 Boot modes
4	If a DHCOR variant with WiFi/BT is used, it is mandatory to connect LPO_IN_32kHz pin on the carrier board design in the correct way. Please have a look at chapter 15.4 32kHz reference clock
5	DH electronics strongly recommends to enable the access to the USB OTG port on the carrier board for flash programming. Please have a look at chapter 21 USB boot and flash programming
6	Please ensure, that VBAT is connected to VCC_IO at the carrier board design, if no external battery is used in the application. Please have a look at chapter 12.1.1 VBAT
7	Ensure, that the Quad SPI NOR-Flash pins are left open at the carrier board design, if a DHCOR variant with Onboard SPI flash is used. Please have a look at chapter 10 Quad SPI NOR-Flash
9	Ensure correct RST# connection. Please have a look at chapter 7 Reset
10	Does the carrier board design provide any serial connection to bootloader and Linux console? Please have a look at chapter 20 UART for bootloader and Linux console

Number	Checklist / Design notes
11	Use Mainboard-HW coding pins for your customer specific mainboard PCB coding. Please have a look at table Table 16: Mainboard-HW coding

Table 23: Hardware design checklist

27 RoHS conformance

This device has been manufactured RoHS II-compliant.