DHCOM STANDARD SPECIFICATION

Specification for the DHCOM standard

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THE ART OF INNOVATION

History

Version	Date	Description or changes	Name
1.1	25/09/2013	Transfer to new template	HH
1.2	14/05/2014	DHCOM-X Standard added	AG
1.3	04/08/2014 10/11/2014	DHCOM-X to Molex SlimStack connector adapted Template error corrected, since it is still the old template	AG SD
1.4	11/12/2014	Add HDMI DDC Information Changed DHCOM-X figures to new dimensions	AG
1.5	10/02/2015	Translation to English	AG
R01	11/17/2016	Missing CS_C, CS_D and CS_E add to table 18 Add VDDA_Audio and VSSA_Audio information to 5.1.12 Digital Audio Add VDDA information to 7.1 power supply Changed comment about i.MX6 Solo and DualLite cooling	AG

Table of contents

1 Abbreviations

- AIN = Analog input
- AINOUT = Analog input/output
- I = Input
- IO = Input/output
- MBC = Must be connected
- O = Output
- PD = Pull-Down
- PU = Pull-Up
- PWR_I = Power input
- PWR_O = Power output
- TBD = To be defined

2 Introduction

2.1 Overview

This DHCOM standard specification defines form, fit and function compatible modules in SODIMM-200 format. All of the hardware and software characteristics for this are defined, from mechanical dimensions to pin assignments and the software development environment.

2.2 Motivation

The DHCOM standard provides a facility for combining different SOC (System-on-Chip) on a module platform. This provides a considerable amount of scalability of the CPU performance of a terminal, without having to adapt the device or the mainboard to a different CPU. The basis of this platform is formed by the SODIMM-200 connector, which is used as standard for all DHCOM and DHCOM-X core modules.

The DHCOM standard defines that certain interface functions are always in the same position at the SODIMM connector. This ensures that the same function is always connected to the same SODIMM pin, even in following CPU modules.

In order to ensure that different voltage levels are supported, different function groups have been combined into supply groups in the DHCOM standard. For each function group there is a reference voltage output which notifies the voltage level of the respective core module to the mainboard hardware. In this way, different voltage levels from different core modules can be balanced using level shifters. These level shifters do not have to be provided for cost-sensitive assemblies, but in this case, the customer may lose the compatibility with the DHCOM standard.

As well as the SODIMM-200 connector, the DHCOM-X standard also provides another facility for contacting high-speed signals such as PCIe. Contacting takes place via an additional Molex high-speed connector on the back of the module. The SODIMM pin assignments are unchanged with the DHCOM-X standard.

Advantages of DHCOM standard:

- Easy core module replacement in an existing mainboard in order to provide more or less computing power.
- Easy way of optimizing costs of an existing assembly by using a newer cost-optimized and performance-optimized CPU.
- Time-optimized and cost-optimized mainboard design, since the interfaces of different terminals are always connected in an identical way, even though different CPUs are being used.
- The operating systems provide uniform interfaces for the DHCOM standard. The cost of porting is therefore reduced considerably for a DHCOM core module.
- Extremely cost-effective connector.

- Compact design.
- If no high-speed signals such as HDMI or PCIe are needed, a DHCOM module can be used instead of a DHCOM-X module in the same mainboard hardware. Costs can therefore be reduced in a simple way.

3 Module overview

3.1 Overview

The interfaces of the DHCOM module series are shown in the following block diagram.

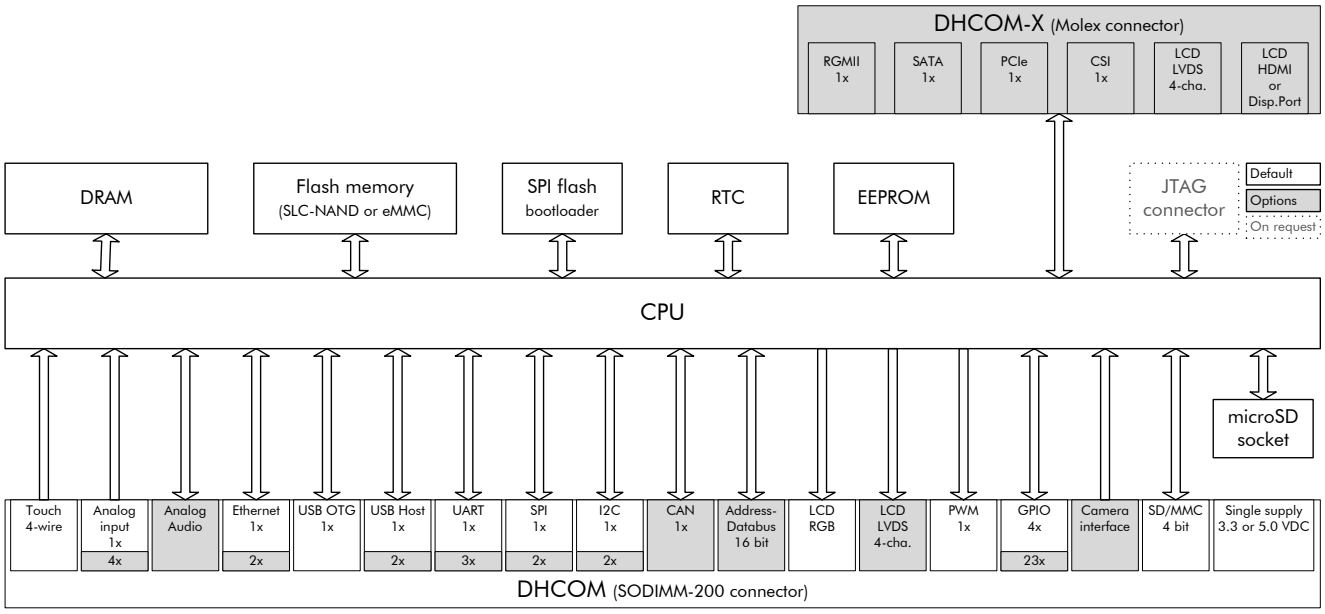

Figure 1: Block diagram

Beside the SODIMM-200 interface, DHCOM-X also offers an additional 80-pin interface on which high-speed signals (HDMI, PCIe etc.) are placed. The DHCOM-X interface is contacted with a special Molex high-speed connector.

A schematic side view of a DHCOM-X core module can be seen in the following figure:

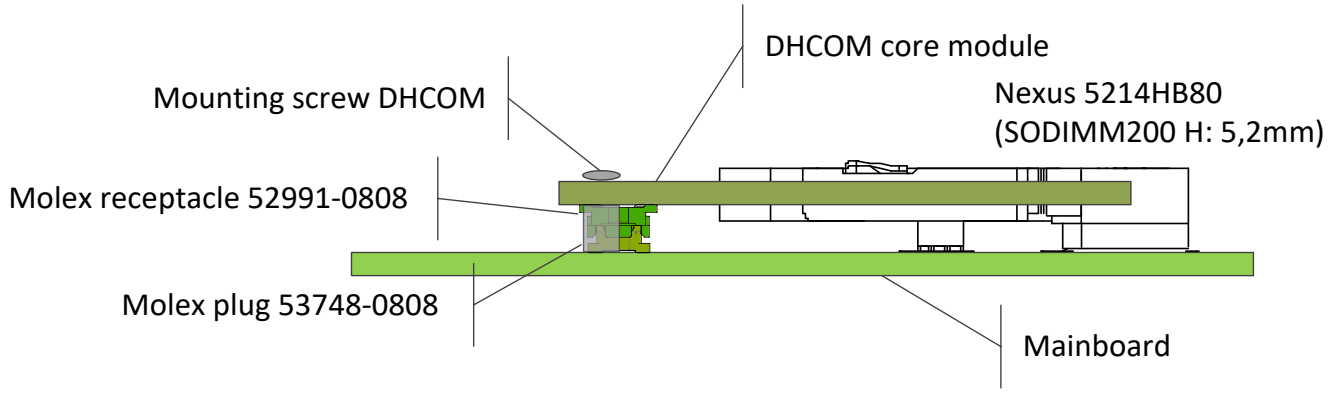

Figure 2: DHCOM-X side view

3.2 Interfaces

The DHCOM specification defines the following interfaces: At least the minimum quantity is always available on each module. The maximum quantity is the number of possible interfaces, which is limited by the number of contacts on the SODIMM-200 and the Molex connector.

Interface	Min. quantity	Max. quantity	Notes	DHCOM Standard
Ethernet	1	2		DHCOM
USB HOST	1	2		DHCOM
USB OTG	1	1		DHCOM
UART	1	3		DHCOM
SPI	1	2		DHCOM
I²C	1	2		DHCOM
CAN	0	1		DHCOM
SDCard	1	1	4 Bit mode	DHCOM
Display	1	1	Min. 16bit; Max. 24bit	DHCOM
Display LVDS	0	1		DHCOM
Touch	1	1	4-wire	DHCOM
Camera	0	1		DHCOM
Audio Input	0	1		DHCOM
Audio Line Out	0	1		DHCOM
Analog Input	1	4		DHCOM
Bus interface	0	1	16bit data bus with 16bit address bus	DHCOM
CS	0	5	Chip select	DHCOM
GPIO	4	23		DHCOM
Interrupt	1	1		DHCOM
PWM Output	1	1		DHCOM
SATA	0	1		DHCOM-X
PCIe	0	1		DHCOM-X
HDMI or DisplayPort	0	1		DHCOM-X
Display LVDS 2nd channel	0	1		DHCOM-X
RGMII	0	1		DHCOM-X
MIPI CSI-2	0	1	Two lane MIPI CSI2-Interface	DHCOM-X

Table 1: DHCOM Interfaces

Note: If only one UART of the possible three is present for a DHCOM core module, for example, the interface is connected to the UART1 pins at the SODIMM socket. In other words, the interface pins with the lowest number are always assigned first.

3.3 Compatibility

Each DHCOM standard module can be used in a mainboard that has been developed with the DHCOM specification in accordance with the form, fit and function compatible motto.

The only restriction is because of the DHCOM-X standard. These core modules are connected via a secondary connector to the mainboard. In addition to that it is necessary to use the 5.2mm high SODIMM-200 socket. However, the SODIMM-200 connector assignment of HDCOM-X is also 100% identical to that of DHCOM.

Furthermore, function groups are specified for DHCOM standard in order to ensure compatibility. Each of these function groups has a reference voltage output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters can therefore be used on the customer hardware to adjust different voltage levels between different DHCOM core modules:

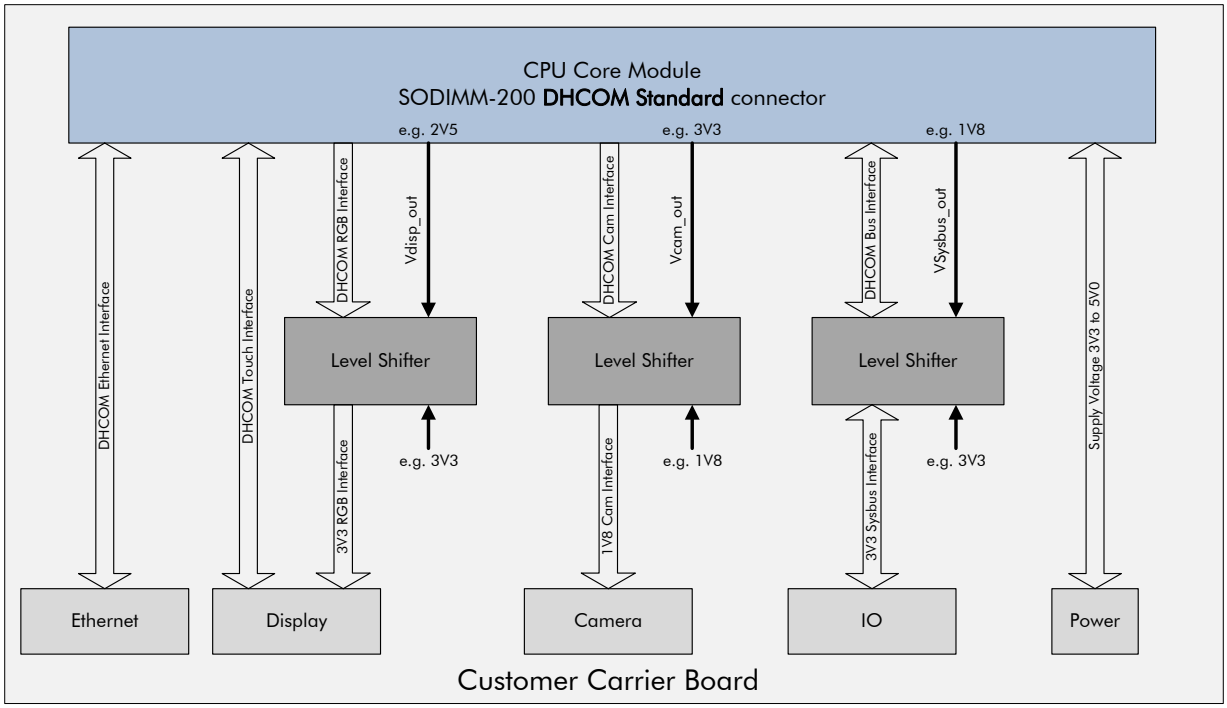

Figure 3: DHCOM function group concept

Of course, a customer can do without these level shifters. However, because of this the customer would probably lose compatibility with another DHCOM core module.

However, at this point it must also be noted that the current voltage level differences between the current DHCOM core modules are extremely small:

Voltage	i.MX25	AM3517	AM335x	i.MX6
VCC (Vin)	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V
Vbat	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V	1.3V – 5.5V
Vsysbus	1.8V	3.3V	3.3V	-
Vdisp	3.3V	3.3V	3.3V	3.3V
Vcam	3.3V	3.3V	3.3V	3.3V
VIO	3.3V	3.3V	3.3V	3.3V
VETH_VIO_SWITCHED	3.3V	3.3V	3.3V	3.3V

Table 2: Voltage groups

Only the the parallel system bus of the i.MX25 is therefore a problem at present.

Furthermore, it is necessary to pay attention if a DHCOM core module is replaced by another, whether all previously used interfaces are present on the new core module. For example, not every DHCOM core module has all three UART interfaces. However, if all three UARTs are needed in the customer hardware, you cannot change to a module that only provides two UARTs.

3.4 Connectors

3.4.1 SODIMM-200 (DHCOM)

A DHCOM standard module is designed for use in a 2.5V DDR2 SODIMM-200 memory socket.

DHCOM-X note: DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector.

The following SODIMM-200 sockets have been tested and approved:

Manufacturer	Description	Article number
Nexus Components http://www.nexus-de.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	DMD-200-RSE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	1473005-1
FCI http://www.fci.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	59354-052FSLF
Nexus Components http://www.nexus-de.com/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	DMD-200-RPE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	1612618-1

Table 3: SODIMM-200 sockets

3.4.2 Molex (DHCOM-X)

A Molex (http://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector. DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

SODIMM-200 socket height	Description	Article number
5.2mm	0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits	Molex 53748-0808
9.2mm	Not available	Not available

Table 4:_ DHCOM-X sockets

3.4.3 JTAG

The JTAG connector is placed on the DHCOM core module and can be contacted with a 10-pin FFC cable.

Manufacturer	Description	Article number
Würth Elektronik http://www.we-online.com	0.50 mm flat flexible cable Type 1 WR-FPC	687 610 050 002
Molex http://www.molex.com/	0.50mm flat flexible cable Type A	982660097

Table 5: FFC Cable

4 Software

4.1 Overview

4.2 Operating systems

4.3 Driver

4.4 Development environment

5 Interface specification

5.1 DHCOM

5.1.1 Power supply

The power supply of the core module is provided via the VIN connections with an extended input range of 3.3V to 5V.

Additional supply inputs are the buffering of the real-time clock and the analogue power supply.

A DHCOM standard module generally has the following power domains:

- Vin = Core module supply voltage input
- Vbat = Battery voltage input
- Vsysbus = System bus voltage output
- Vdisp = Display voltage output
- Vcam = Camera voltage output
- VIO = I/O voltage output
- VDDA = Analog Audio supply voltage input = 3,3V

The assignment of Power domain to SODIMM-200 socket pin can be found in table Table 33 on page 34.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
VCC_IN1	Core Module supply voltage input	38	PWR_I	MBC
VCC_IN2	Core Module supply voltage input	39	PWR_I	MBC
VCC_IN3	Core Module supply voltage input	40	PWR_I	MBC
VCC_IN4	Core Module supply voltage input	41	PWR_I	MBC
VCC_IN5	Core Module supply voltage input	42	PWR_I	MBC
VCC_IN6	Core Module supply voltage input	44	PWR_I	MBC
GND1	Core Module Ground	17	PWR_I	MBC
GND2	Core Module Ground	19	PWR_I	MBC
GND3	Core Module Ground	43	PWR_I	MBC
GND4	Core Module Ground	45	PWR_I	MBC
GND5	Core Module Ground	47	PWR_I	MBC
GND6	Core Module Ground	101	PWR_I	MBC
GND7	Core Module Ground	111	PWR_I	MBC
GND8	Core Module Ground	153	PWR_I	MBC
GND9	Core Module Ground	185	PWR_I	MBC
GND10	Core Module Ground	199	PWR_I	MBC
VCC_BAT	Core Module Battery voltage input	200	PWR_I	MBC
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	MBC
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-
Vcam_OUT	Camera supply voltage output	102	PWR_O	-
VIO_OUT	I/O supply voltage output	152	PWR_O	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
RESET_IN	System Reset input (active low)	21	I	-
RESET_OUT	System Reset output (active low)	20	O	-

Table 6: Power supply and reset

5.1.2 Touch

The DHCOM touch interface is a 4-wire resistive touch interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
TSPX	Resistive Touch: 4 wire (X +)	12	AINOUT	PD
TSMX	Resistive Touch: 4 wire (X -)	14	AINOUT	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	AINOUT	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	AINOUT	PD

Table 7: Resistiv Touch

5.1.3 Analog Input

The DHCOM standard provides four analogue inputs. Additional functions can be realised using the analogue inputs. For example, these are voltage monitoring of important supplies, depending on the module. These functions can be found in the associated "user manual".

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
AD0	Analog input 0	8	AIN	PD
AD1	Analog input 1	6	AIN	PD
AD2	Analog input 2	4	AIN	PD
AD3	Analog input 3	2	AIN	PD

Table 8: Analog Input

5.1.4 Ethernet

The DHCOM standard provides two Ethernet ports. Only the transformer for galvanic separation is required on the mainboard side. Outputs for an LED for the existing link and an LED for speed indication are provided. IO voltage is also provided in order to switch the transformer into a kind of suspend mode for energy-saving purposes.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
ETH_VIO_SWITCHED	Analogue power supply output to magnetics	194	PWR_O	-
nETH1_LINK_LED	Port 1: Activity LED connection	186	O	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	O	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	O	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	O	PD
ETH1_RXI-	Port 1: Ethernet TX Differential Input (minus)	196	I	PD
ETH1_RXI+	Port 1: Ethernet TX Differential Input (plus)	198	I	PD
nETH2_LINK_LED	Port 2: Activity LED connection	187	O	PD
nETH2_SPEED_LED	Port 2: Speed LED connection	189	O	PU
ETH2_TXD-	Port 2: Ethernet TX Differential Output (minus)	191	O	PD
ETH2_TXD+	Port 2: Ethernet TX Differential Output (plus)	193	O	PD

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
ETH2_RXI-	Port 2: Ethernet TX Differential Input (minus)	195	I	PD
ETH2_RXI+	Port 2: Ethernet TX Differential Input (plus)	197	I	PD

Table 9: Ethernet

5.1.5 USB OTG

The DHCOM standard provides a USB OTG interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
USB_OTG_VBUS	OTG Client: VBUS Input line OTG Host: USB bus supply voltage	166	I / PWR_O	PD
USB_OTG_ID	OTG ID Pin: Connected to the OTG Mini-AB connector (Micro-A: ID-Pin = GND → Host / Micro-B: ID-Pin = floating → Client)	168	I	-
USB_OTG_D+	USB OTG differential Signal positive line	170	IO	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	IO	PD

Table 10: USB OTG

Note: The DHCOM USB OTG port does not provide any "enable" or "over current" signal. For this reason, the USB OTG ID pin must be used for switching the 5V USB voltage on and off. An overcurrent event can be detected by a customer with one of the free DHCOM GPIOs. However, this functionality is not supported by the standard driver.

5.1.6 USB Host

The DHCOM standard provides two USB Host interfaces.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
USB_PWR_STAT	USB Host over current indicator (active low)	174	I	-
USB_PWR_EN	USB Host power enable signal (active low)	176	O	-
USB_HOST1_D+	USB Host 1 differential Signal positive line	178	IO	PD
USB_HOST1_D-	USB Host 1 differential Signal negative line	180	IO	PD
USB_HOST2_D+	USB Host 2 differential Signal positive line	169	IO	PD
USB_HOST2_D-	USB Host 2 differential Signal negative line	171	IO	PD

Table 11: USB Host

Note: The two DHCOM Host ports share the "enable" and "over current" signals.

5.1.7 UART

The DHCOM standard provides three UART interfaces.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
UART1_DTR	Full function UART data terminal ready	22	O	-
UART1_CTS	UART clear to send	24	I	-
UART1_RTS	UART request to send	26	O	-
UART1_DSR	Full function UART data set ready	28	I	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
UART1_DCD	Full function UART data carrier detect	30	I	-
UART1_RX	UART receive data line	32	I	-
UART1_TX	UART transmit data line	34	O	-
UART1_RI	Full function UART ring indicator	36	I	-
UART2_CTS	UART clear to send	31	I	-
UART2_RTS	UART request to send	33	O	-
UART2_RX	UART receive data line	35	I	-
UART2_TX	UART transmit data line	37	O	-
UART3_RX	Serial port receive data line	23	I	-
UART3_TX	Serial port transmit data line	25	O	-

Table 12: UART

5.1.8 SPI

The DHCOM standard provides two SPI interfaces.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
SPI1_CS0	SPI 1 Slave select signal	177	O	-
SPI1_CLK	SPI 1 clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	179	IO	-
SPI1_MISO	SSP 1 receive data line	181	I	-
SPI1_MOSI	SSP 1 transmit data line	183	O	-
SPI2_CS0	SPI 2 Slave select signal	155	O	-
SPI2_CLK	SPI 2 clock line. Can be configured as an output (master-mode operation) or an input (slave-mode operation)	157	IO	-
SPI2_MISO	SSP 2 receive data line	159	I	-
SPI2_MOSI	SSP 2 transmit data line	161	O	-

Table 13: SPI

5.1.9 I²C™

The DHCOM standard provides two I²C™ interfaces.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
I2C1_CLK	I²C 1 clock line	182	IO	-
I2C1_DATA	I²C 1 data line	184	IO	-
I2C2_CLK	I²C 2 clock line	158	IO	-
I2C2_DATA	I²C 2 data line	160	IO	-

Table 14: I²C™

Note: I2C1 can be used for HDMI DDC (Display Data Channel).

5.1.10 CAN

The DHCOM standard provides a CAN interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
CAN_TX	CAN transmit data line	27	IO	-
CAN_RX	CAN receive data line	29	IO	-

Table 15: CAN

5.1.11 Analog Audio

The DHCOM standard provides analogue Line-In and Mic-In inputs and a headphone output. The supply voltage for the analogue area has to be generated externally and placed onto the SODIMM socket in order to be able to optimise the filter quality.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	MBC
MIC_IN	Microphone Input Signal	1	I	PD
MIC_GND	Microphone Ground	3	PWR_I	-
LINEIN_L	Line-In Left	5	I	PD
LINEIN_R	Line-In Right	7	I	PD
HP_GND	Headphone Ground	11	PWR_O	-
HP_OUT_LEFT	Headphone Output left	13	O	-
HP_OUT_RIGHT	Headphone Output right	15	O	-

Table 16: Analog Audio

5.1.12 Digital Audio (I2S)

The DHCOM standard provides a facility for alternatively placing the digital I2S interface on the analogue audio signals. The standard interface is therefore available on these pins for connecting an audio codec.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
VDDA_Audio	Audio Codec supply voltage input	10	PWR_I	MBC
VSSA_Audio	Audio Codec Ground	9	PWR_I	MBC
I2S_RXFS	Receive Frame sync signal	1	I	PD
I2S_RXD	Data receive signal	5	I	PD
I2S_RXC	Receive clock signal	7	I	PD
I2S_TXFS	Transmit Frame sync signal	11	O	-
I2S_TXD	Data transmit signal	15	O	-
I2S_TXC	Transmit clock signal	13	O	-

Table 17: I2S

5.1.13 Address and data bus

The DHCOM standard provides a parallel system bus.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
Vsysbus_OUT	System bus supply voltage output	110	PWR_O	-
A00	Memory controller address line	113	O	-
A01	Memory controller address line	115	O	-
A02	Memory controller address line	117	O	-
A03	Memory controller address line	119	O	-
A04	Memory controller address line	121	O	-
A05	Memory controller address line	123	O	-
A06	Memory controller address line	125	O	-
A07	Memory controller address line	127	O	-
A08	Memory controller address line	112	O	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
A09	Memory controller address line	114	O	-
A10	Memory controller address line	116	O	-
A11	Memory controller address line	118	O	-
A12	Memory controller address line	120	O	-
A13	Memory controller address line	122	O	-
A14	Memory controller address line	124	O	-
A15	Memory controller address line	126	O	-
D00	Memory controller data line	135	IO	-
D01	Memory controller data line	137	IO	-
D02	Memory controller data line	139	IO	-
D03	Memory controller data line	141	IO	-
D04	Memory controller data line	143	IO	-
D05	Memory controller data line	145	IO	-
D06	Memory controller data line	147	IO	-
D07	Memory controller data line	149	IO	-
D08	Memory controller data line	136	IO	-
D09	Memory controller data line	138	IO	-
D10	Memory controller data line	140	IO	-
D11	Memory controller data line	142	IO	-
D12	Memory controller data line	144	IO	-
D13	Memory controller data line	146	IO	-
D14	Memory controller data line	148	IO	-
D15	Memory controller data line	150	IO	-
CS_A	Static memory chip select 0	128	O	-
CS_B	Static memory chip select 1	129	O	-
CS_C	Static memory chip select 1	130	O	-
CS_D	Static memory chip select 1	131	O	-
CS_E	Static memory chip select 1	132	O	-
WE	Memory controller write enable	133	O	-
OE	Memory controller output enable	134	O	-

Table 18: Address and data bus

5.1.14 RGB Display

The DHCOM standard provides a parallel 24-bit RGB interface for driving displays.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
Vdisp_OUT	LCD controller supply voltage output	46	PWR_O	-
LC_R0	LCD display data red 0	76	O	-
LC_R1	LCD display data red 1	78	O	-
LC_R2	LCD display data red 2	49	O	-
LC_R3	LCD display data red 3	51	O	-
LC_R4	LCD display data red 4	53	O	-
LC_R5	LCD display data red 5	55	O	-
LC_R6	LCD display data red 6	57	O	-
LC_R7	LCD display data red 7	59	O	-
LC_G0	LCD display data green 0	80	O	-
LC_G1	LCD display data green 1	82	O	-
LC_G2	LCD display data green 2	61	O	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
LC_G3	LCD display data green 3	63	O	-
LC_G4	LCD display data green 4	65	O	-
LC_G5	LCD display data green 5	67	O	-
LC_G6	LCD display data green 6	69	O	-
LC_G7	LCD display data green 7	71	O	-
LC_B0	LCD display data blue 0	84	O	-
LC_B1	LCD display data blue 1	86	O	-
LC_B2	LCD display data blue 2	73	O	-
LC_B3	LCD display data blue 3	75	O	-
LC_B4	LCD display data blue 4	77	O	-
LC_B5	LCD display data blue 5	79	O	-
LC_B6	LCD display data blue 6	81	O	-
LC_B7	LCD display data blue 7	83	O	-
LC_EN	LCD display enable	85	O	-
LC_VSYNC	LCD frame or vertical sync. puls	87	O	-
LC_HSYNC	LCD line or horizontal sync. puls	89	O	-
LC_PCLK	LCD pixel clock	91	O	-
GPIO_PWM	LCD contrast (only if PWM is not used)	100	O	-

Table 19: RGB Interface

5.1.15 LVDS

The DHCOM standard provides an LVDS channel for driving displays.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
LVDS_TX0+	LVDS channel 0 differential data output positive line	88	O	-
LVDS_TX0-	LVDS channel 0 differential data output negative line	90	O	-
LVDS_TX1+	LVDS channel 1 differential data output positive line	92	O	-
LVDS_TX1-	LVDS channel 1 differential data output negative line	94	O	-
LVDS_TX2+	LVDS channel 2 differential data output positive line	93	O	-
LVDS_TX2-	LVDS channel 2 differential data output negative line	95	O	-
LVDS_TX3+	LVDS channel 3 differential data output positive line	96	O	-
LVDS_TX3-	LVDS channel 3 differential data output negative line	98	O	-
LVDS_CLK+	LVDS differential clock output positive line	97	O	-
LVDS_CLK-	LVDS differential clock output negative line	99	O	-

Table 20: LVDS

Note: A second LVDS channel is available with the DHCOM-X standard.

5.1.16 Camera parallel

The DHCOM standard provides a parallel 10-bit camera interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
CIF_HSYNC	CSI Interface Line Synchronization	74	IO	-
CIF_PCLK	CSI Interface Pixel Clock input	72	IO	-
CIF_MCLK	CSI Interface Master Clock output	70	IO	-
CIF_VSYNC	CSI Interface Frame Synchronization	68	IO	-
CIF_D9	CSI Interface Data line 9	66	IO	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
CIF_D8	CSI Interface Data line 8	64	IO	-
CIF_D7	CSI Interface Data line 7	62	IO	-
CIF_D6	CSI Interface Data line 6	60	IO	-
CIF_D5	CSI Interface Data line 5	58	IO	-
CIF_D4	CSI Interface Data line 4	56	IO	-
CIF_D3	CSI Interface Data line 3	54	IO	-
CIF_D2	CSI Interface Data line 2	52	IO	-
CIF_D1	CSI Interface Data line 1	50	IO	-
CIF_D0	CSI Interface Data line 0	48	IO	-
Vcam_OUT	Voltage for external Level-Shifter	102	PWR_O	-

Table 21: Camera parallel

Note: The camera interface pins can also optionally be used as GPIOs. This functionality is also supported by the operating systems.

5.1.17 PWM

The DHCOM standard provides a PWM output.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
GPIO_PWM	PWM channel (only if LCD contrast is not used)	100	O	-

Table 22: PWM

5.1.18 SD / SDIO / MMC

The DHCOM standard provides a 4-bit SD / SDIO / MMC interface.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
SD_CLK	SD/SDIO/MMC bus clock	103	O	-
SD_CMD	SD/SDIO/MMC command line	104	IO	-
SD_DETECT	SD/SDIO/MMC card detection(active high)	105	I	PD
SD_D0	SD/SDIO/MMC data line	106	IO	-
SD_D1	SD/SDIO/MMC data line	107	IO	-
SD_D2	SD/SDIO/MMC data line	108	IO	-
SD_D3	SD/SDIO/MMC data line	109	IO	-

Table 23: SD / SDIO / MMC

5.1.19 GPIO

The DHCOM standard provides freely usable GPIOs. These also include the camera interface pins.

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	IO	PU
GPIO _A	General Purpose I/O	154	IO	-
GPIO _B	General Purpose I/O	156	IO	-
GPIO _C	General Purpose I/O	162	IO	-
GPIO _D	General Purpose I/O	163	IO	-
GPIO _E	General Purpose I/O	164	IO	-

SODIMM pin name	Description	SODIMM pin number	IO Type	Not used
GPIO _F	General Purpose I/O	165	IO	-
GPIO _G	General Purpose I/O	167	IO	-
GPIO _H	General Purpose I/O	173	IO	-
GPIO _I	General Purpose I/O	175	IO	-
VIO_OUT	Voltage for external Level-Shifter	152	PWR_O	-
GPIO_J (or CIF_HSYNC)	General Purpose I/O	74	IO	-
GPIO_K (or CIF_PCLK)	General Purpose I/O	72	IO	-
GPIO_L (or CIF_MCLK)	General Purpose I/O	70	IO	-
GPIO_M (or CIF_VSYNC)	General Purpose I/O	68	IO	-
GPIO_N (or CIF_D9)	General Purpose I/O	66	IO	-
GPIO_O (or CIF_D8)	General Purpose I/O	64	IO	-
GPIO_P (or CIF_D7)	General Purpose I/O	62	IO	-
GPIO_Q (or CIF_D6)	General Purpose I/O	60	IO	-
GPIO_R (or CIF_D5)	General Purpose I/O	58	IO	-
GPIO_S (or CIF_D4)	General Purpose I/O	56	IO	-
GPIO_T (or CIF_D3)	General Purpose I/O	54	IO	-
GPIO_U (or CIF_D2)	General Purpose I/O	52	IO	-
GPIO_V (or CIF_D1)	General Purpose I/O	50	IO	-
GPIO_W (or CIF_D0)	General Purpose I/O	48	IO	-
Vcam_OUT	Voltage for external Level-Shifter	102	PWR_O	-

Table 24: GPIOs

5.2 DHCOM-X

5.2.1 RGMII

The DHCOM-X connector provides an RGMII interface. This is the standard interface between Ethernet MAC and PHY for Gbit Ethernet.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
RGMII_TXCLK	RGMII transmit clock, 125 MHz digital	2	O	Vrgmii	-
RGMII_TXD0	RGMII transmit data 0	4	O	Vrgmii	-
RGMII_TXD1	RGMII transmit data 1	6	O	Vrgmii	-
RGMII_TXD2	RGMII transmit data 2	8	O	Vrgmii	-
RGMII_TXD3	RGMII transmit data 3	10	O	Vrgmii	-
RGMII_TX_CTL	RGMII transmit enable	12	O	Vrgmii	-
RGMII_RXCLK	RGMII receive clock, 125 MHz digital	1	I	Vrgmii	-
RGMII_RXD0	RGMII received data 0	3	I	Vrgmii	-
RGMII_RXD1	RGMII received data 1	5	I	Vrgmii	-
RGMII_RXD2	RGMII received data 2	7	I	Vrgmii	-
RGMII_RXD3	RGMII received data 3	9	I	Vrgmii	-
RGMII_RX_CTL	RGMII receive data valid	11	I	Vrgmii	-
RGMII_MDC	Management data clock	14	O	Vrgmii	-
RGMII_MDIO	Management data	13	IO	Vrgmii	-
RGMII_REFCLK	MAC reference clock input (125MHz)	16	I	Vrgmii	-
RGMII_RST	PHY reset	15	O	Vrgmii	-
RGMII_INT	PHY interrupt (active low)	18	I	3V3	PU
RGMII_WOL_INT	PHY Wake-on-LAN interrupt (active low)	17	I	3V3	PU

VCC_RGMII_OUT	Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	Vrgmii	-

Table 25: RGMII

5.2.2 SATA

The DHCOM-X connector provides a serial ATA (SATA, also S-ATA/Serial Advanced Technology Attachment) interface.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
SATA_TX+	SATA transmit data positive	24	O	Sata	-
SATA_TX-	SATA transmit data negative	26	O	Sata	-
SATA_RX+	SATA receive data positive	21	I	Sata	-
SATA_RX-	SATA receive data negative	23	I	Sata	-

Table 26: Sata

5.2.3 PCIe

The DHCOM-X connector provides a "Peripheral Component Interconnect Express" interface.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
PCIE_RX+	PCIe receive data positive	27	I	PCIe	-
PCIE_RX-	PCIe receive data negative	29	I	PCIe	-
PCIE_TX+	PCIe transmit data positive	31	O	PCIe	-
PCIE_TX-	PCIe transmit data negative	33	O	PCIe	-
PCIE_REFCLK+	PCIe 100MHz reference clock output positive	30	O	PCIe	-
PCIE_REFCLK-	PCIe 100MHz reference clock output negative	32	O	PCIe	-
PCIE_WAKE	PCIe wake signal (active low)	34	I	3V3	PU

Table 27: PCIe

5.2.4 MIPI CSI-2

The DHCOM-X connector provides a Camera Serial Interface (CSI-2 spec. from MIPI Alliance).

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
CSI_D0+	CSI received data 0 positive	38	I	CSI	-
CSI_D0-	CSI received data 0 negative	40	I	CSI	-
CSI_D1+	CSI received data 1 positive	42	I	CSI	-
CSI_D1-	CSI received data 1 negative	44	I	CSI	-
CSI_CLK+	CSI reference clock positive	37	I	CSI	-
CSI_CLK-	CSI reference clock negative	39	I	CSI	-

Table 28: MIPI CSI-2

5.2.5 HDMI oder Display Port

The DHCOM-X connector provides a High Definition Multimedia interface. As an alternative to HDMI, a display port interface can also be placed onto these pins.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
HDMI_D0+ DP_Lane0+	HDMI or DP differential data lane 0 positive	48	O	HDMI or DP	-
HDMI_D0- DP_Lane0-	HDMI or DP differential data lane 0 negative	50	O	HDMI or DP	-
HDMI_D1+ DP_Lane1+	HDMI or DP differential data lane 1 positive	52	O	HDMI or DP	-
HDMI_D1- DP_Lane1-	HDMI or DP differential data lane 1 negative	54	O	HDMI or DP	-
HDMI_D2+ DP_Lane2+	HDMI or DP differential data lane 2 positive	47	O	HDMI or DP	-
HDMI_D2- DP_Lane2-	HDMI or DP differential data lane 2 negative	49	O	HDMI or DP	-
HDMI_CLK+ DP_Lane3+	HDMI differential clock positive	43	O	HDMI or DP	-
HDMI_CLK- DP_Lane3-	HDMI differential clock negative	45	O	HDMI or DP	-
HDMI_CEC_IN	HDMI consumer electronic control	51	IO	2V5	-
HDMI_HPD DP_HPD	HDMI or DP hot plug detect	56	I	2V5	-

Table 29: HDMI

Note: For HDMI DDC (Display Data Channel) DHCOM I2C1 must be used (SODIMM-200 pins 182 and 184).

5.2.6 LVDS

The DHCOM-X connector provides a second LVDS channel.

DHCOM-X pin name	Description	DHCOM-X pin number	IO Type	Voltage level	Not used
LVDS2_TX0+	LVDS 2 differential data lane 0 positive	60	O	LVDS	-
LVDS2_TX0-	LVDS 2 differential data lane 0 negative	62	O	LVDS	-
LVDS2_TX1+	LVDS 2 differential data lane 1 positive	64	O	LVDS	-
LVDS2_TX1-	LVDS 2 differential data lane 1 negative	66	O	LVDS	-
LVDS2_TX2+	LVDS 2 differential data lane 2 positive	59	O	LVDS	-
LVDS2_TX2-	LVDS 2 differential data lane 2 negative	61	O	LVDS	-
LVDS2_TX3+	LVDS 2 differential data lane 3 positive	63	O	LVDS	-
LVDS2_TX3-	LVDS 2 differential data lane 3 negative	65	O	LVDS	-
LVDS2_CLK+	LVDS 2 differential clock positive	55	O	LVDS	-
LVDS2_CLK-	LVDS 2 differential clock negative	57	O	LVDS	-

Table 30: LVDS2

6 Mechanical specification

6.1 Overview

The mechanical dimensions of the DHCOM standard module were specified on the basis of systematic analyses of the space required for a modern SoC CPU.

6.2 Dimensions

6.2.1 DHCOM

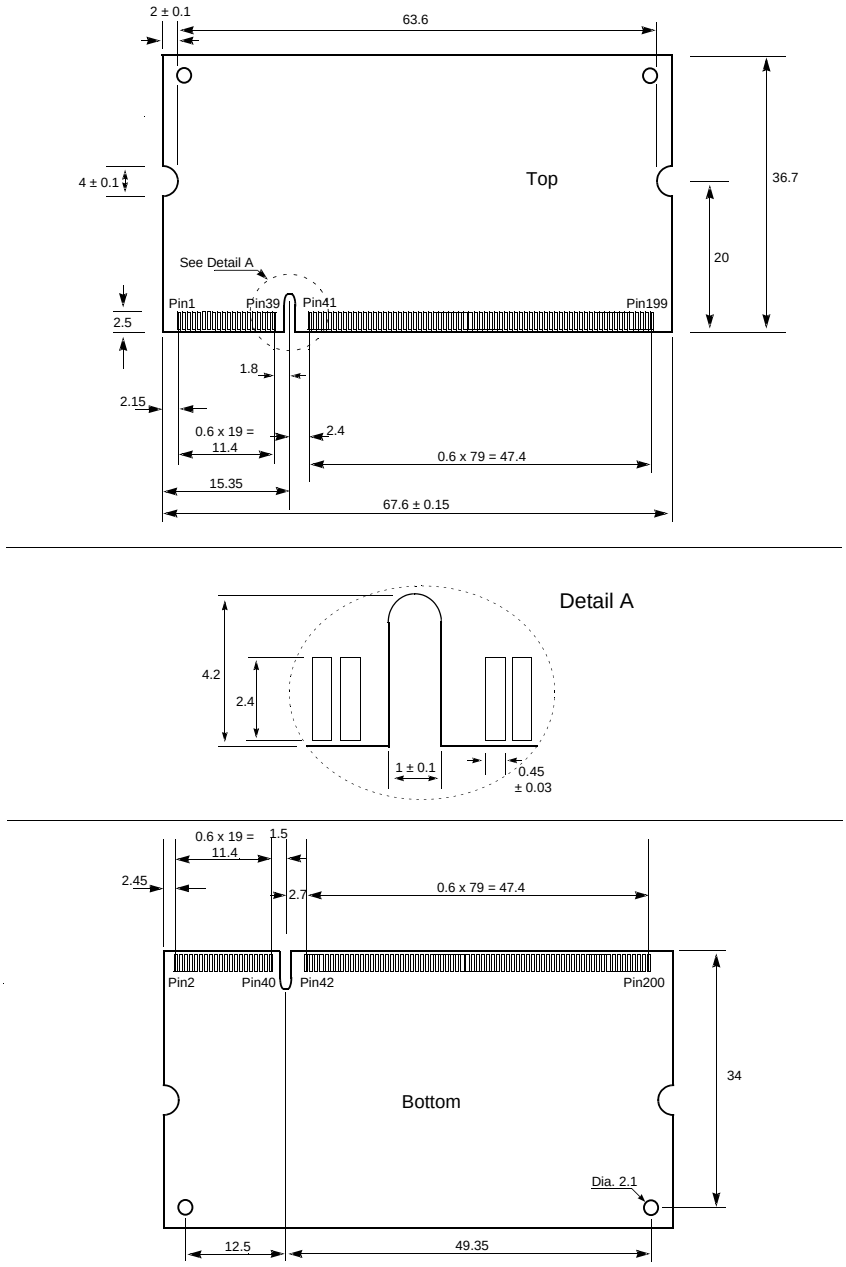

Figure 4: DHCOM dimensions

6.2.2 DHCOM-X

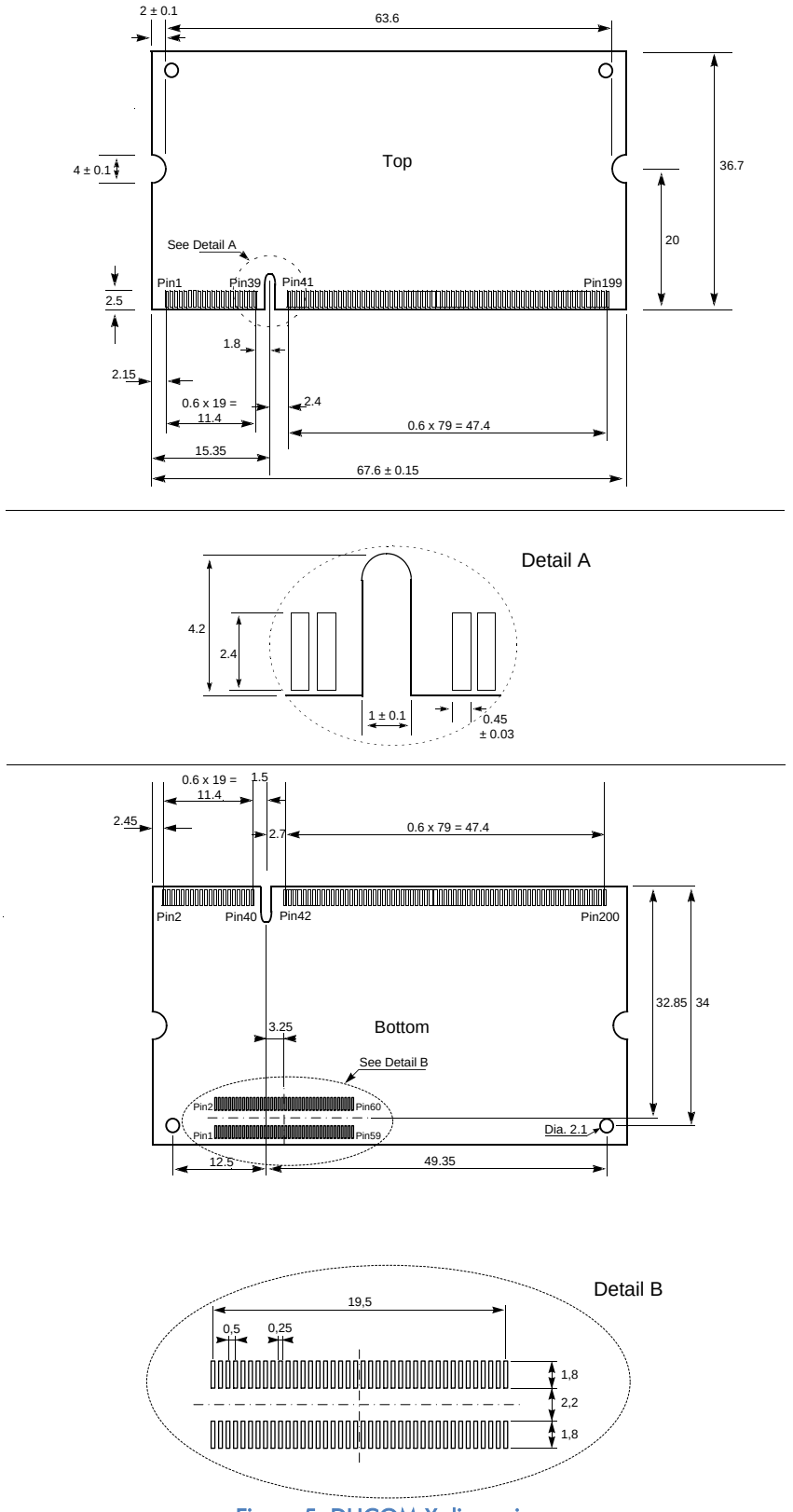

Figure 5: DHCOM-X dimensions

6.3 Connector positioning

In order to be able to guarantee the contacting of both connectors with DHCOM-X, the components must be positioned in exact distance from each other on the mainboard. The following figure shows the dimensions that must be exactly used:

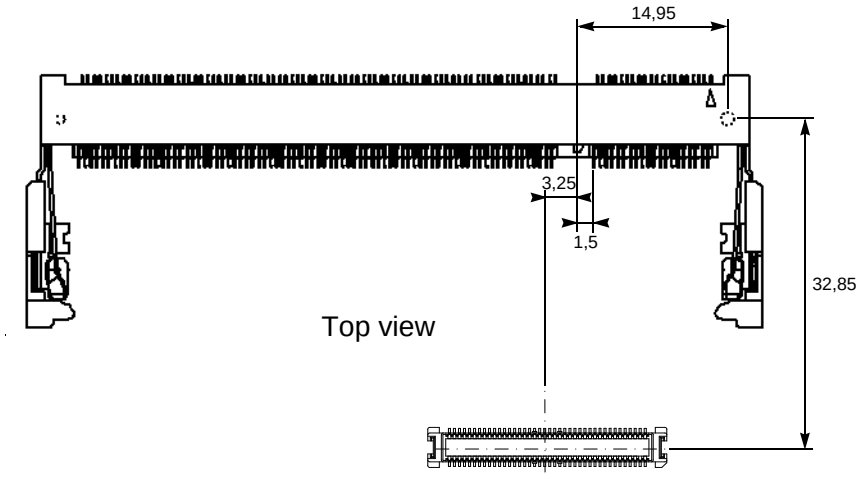

Figure 6: DHCOM-X connector positioning

6.4 Mounting below the DHCOM module

If a SODIMM-200 socket with a height of 5.2 mm is used, components with a maximum height of 1 mm may be mounted below the core module. If the 9.2 mm high socket is used, the maximum component height increases to 5 mm. An example is shown in the following drawing:

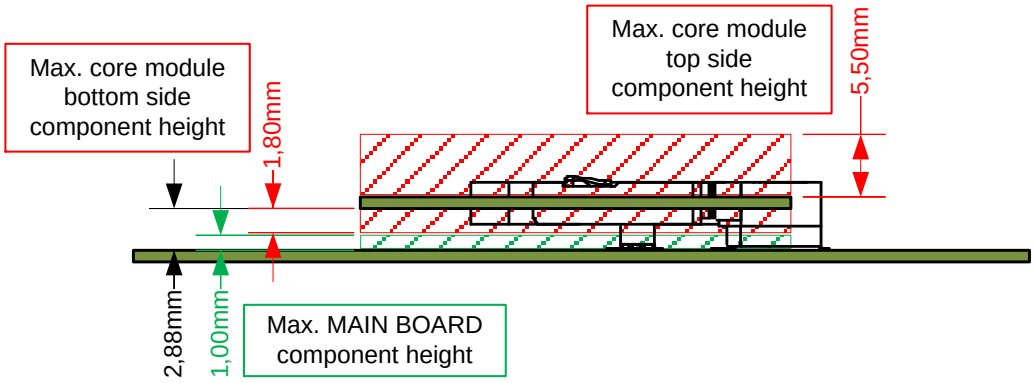

Table 31: Maximum component height

6.5 Mounting

6.5.1 DHCOM

With a DHCOM standard module, attachment with screws is not necessary, but can take place using the following holes for special usage cases:

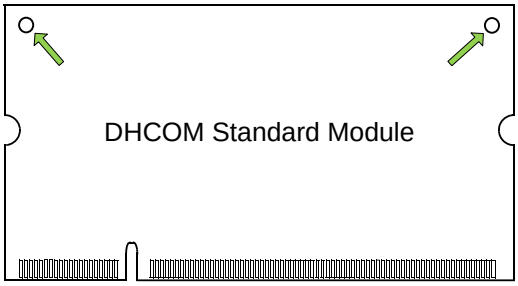

Figure 7: DHCOM attachment

6.5.2 DHCOM-X

With a DHCOM-X core module, attachment is needed in order to ensure that the contacting of the Molex connector is provided, i.e. it must be screwed on at the attachment points (see locations marked in red in the next drawing).

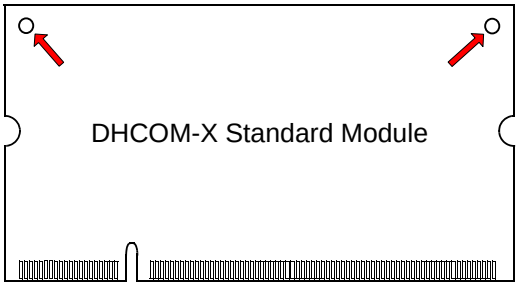

Figure 8: DHCOM-X attachment

6.6 Cooling concept

This chapter relates to the DHCOM core module, which needs to be cooled during operation.

DHCOM CPU Module	Cooling necessary?
i.MX25x	No
AM35x	No
AM335x	No
i.MX6 Solo	**Depends on application**
i.MX6 DualLite	**Depends on application**
i.MX6 Dual	**Yes**
i.MX6 Quad	**Yes**

Table 32: Cooling necessary?

Modern multi-core CPUs such as the i.MX6 from Freescale must have passive cooling. This results in the following problems:

- Heat sink is required
- Heat sink must be assembled on the hardware
- Additional material and manufacturing costs

For this reason, DH electronics GmbH uses an innovative cooling concept that is intended to avoid the above-mentioned disadvantages.

6.6.1 Description

The DHCOM product family is an ARM CPU module family based on SODIMM-200. This means that a DDR2 memory socket with a 2.5V key is used. These sockets are available in different heights:

- 4.0mm
- **5.2mm (Standard product)**
- 8.0mm
- 9.2mm

The 5.2 mm high socket is used for the DHCOM cooling concept. In this case, the CPU does not sit on the top of the PCB like it did before, but on the bottom.

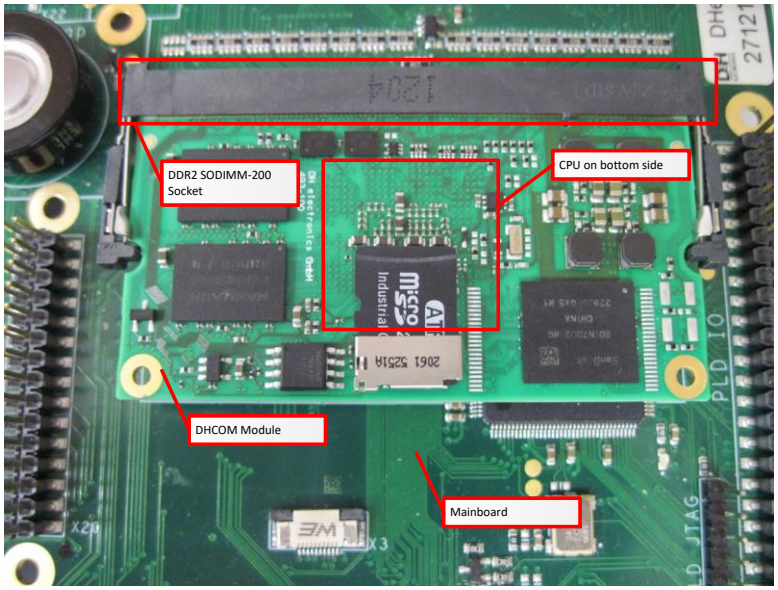

Figure 9: Cooling concept

If the 5.2 mm high SODIMM-200 socket is used, there is a distance of 0.8 mm up to 1.8 mm between the CPU and the mainboard (Depends on CPU housing type). This distance can be bridged with a gap or copper pad for transporting heat. The heat from the CPU is therefore transferred to the mainboard. On the mainboard there are now two ways of distributing the heat with thermal vias:

1. **Dissipation into the inner layers (VCG and GND)**

   The heat is led into the inner layers of a PCB (min. 4 layer PCB) via thermal vias. These inner layers are flooded with copper. Typically, a connection is made to the GND or VCC supply. The entire PCB heats up via these copper planes and therefore gives off the CPU heat into the surrounding area.

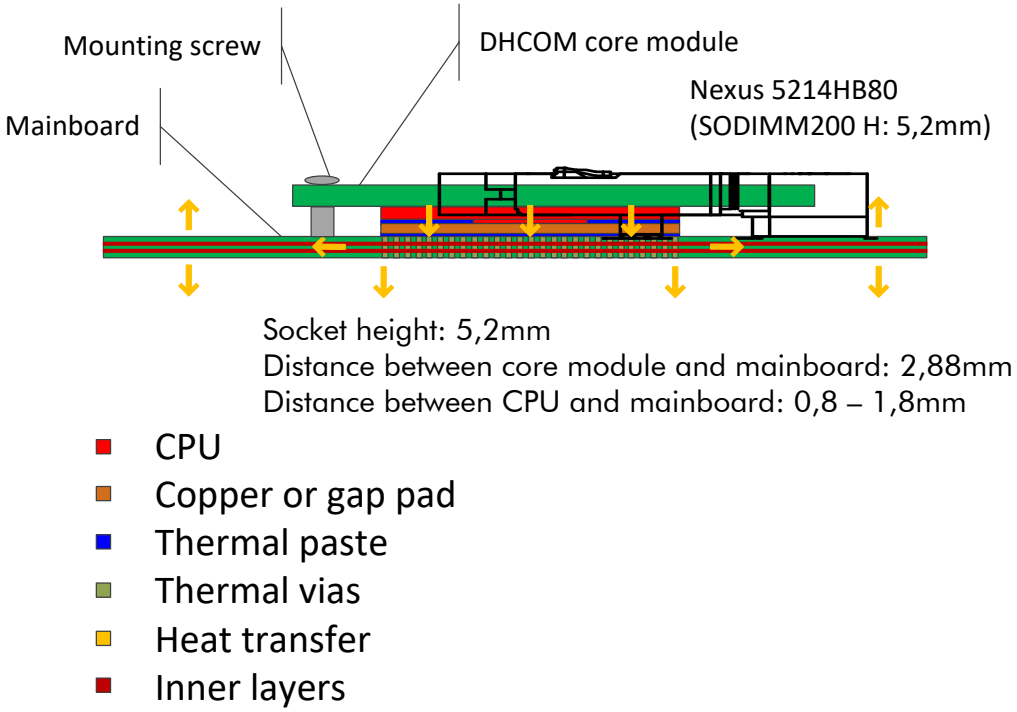

Figure 10: Cooling concept - dissipation into the inner layers

2. **Dissipation on the rear of the mainboard**

If housing is available in the final application on which the heat can be dissipated, it would be possible to lead the heat to the bottom of the mainboard PCB (thermal vias) and dissipate it with an aluminum or copper block to the housing.

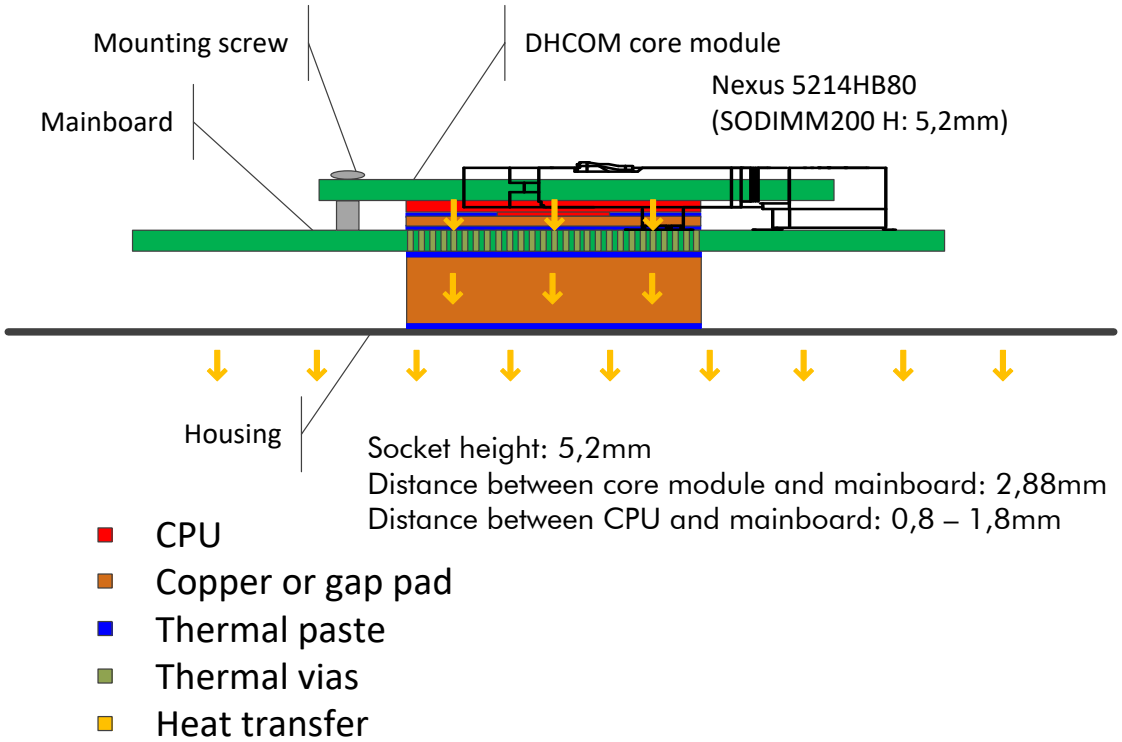

Figure 11: Cooling concept - dissipation on the rear of the mainboard

6.6.2 Advantages

- No heat sink required
- Extremely simple assembly
- Low costs (gap or copper pad and CPU module screw connection required; in the case of dissipation via the housing, a simple aluminum or copper block may be needed)

6.6.3 Conditions required

- The mainboard must have at least 4 layers with large ground and VCC surfaces.
- The copper layer must be large enough to make heat dissipation possible.

6.6.4 Competitors

- Special heat sinks are soldered on → expensive and complicated processing.
- Standard heat sinks are screwed to the CPU module → extremely complicated assembly.

6.7 Pin assignments

6.7.1 SODIMM-200

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
1	Microphone In (or I2S_RXFS)	VDDA	2	Analog Input 3	VDDA
3	Microphone GND	VDDA	4	Analog Input 2	VDDA
5	Line-In Left (or I2S_RXD)	VDDA	6	Analog Input 1	VDDA
7	Line-In Right (or I2S_RXC)	VDDA	8	Analog Input 0	VDDA
9	VSSA (Audio Supply GND)	VDDA	10	VDDA (Audio Supply VCC)	VDDA
11	Headphone GND (or I2S_TXFS)	VIO	12	TSPX	VDDA
13	Headphone Left (or I2S_TXC)	VDDA	14	TSMX	VDDA
15	Headphone Right (or I2S_TXD)	VDDA	16	TSMY	VDDA
17	GND1	Vin	18	TSPY	VDDA
19	GND2	Vin	20	RESET_OUT	VIO
21	RESET_IN	VIO	22	UART1_DTR	VIO
23	UART3_RX	VIO	24	UART1_CTS	VIO
25	UART3_TX	VIO	26	UART1_RTS	VIO
27	CAN_TX	VIO	28	UART1_DSR	VIO
29	CAN_RX	VIO	30	UART1_DCD	VIO
31	UART2_CTS	VIO	32	UART1_RX	VIO
33	UART2_RTS	VIO	34	UART1_TX	VIO
35	UART2_RX	VIO	36	UART1_RI	VIO
37	UART2_TX	VIO	38	VCC_IN1	Vin
39	VCC_IN2	Vin	40	VCC_IN3	Vin
41	VCC_IN4	Vin	42	VCC_IN5	Vin
43	GND3	Vin	44	VCC_IN6	Vin
45	GND4	Vin	46	Vdisp_OUT	Vdisp
47	GND5	Vin	48	GPIO_W (or CIF_D0)	Vcam
49	LC_R2	Vdisp	50	GPIO_V (or CIF_D1)	Vcam
51	LC_R3	Vdisp	52	GPIO_U (or CIF_D2)	Vcam
53	LC_R4	Vdisp	54	GPIO_T (or CIF_D3)	Vcam
55	LC_R5	Vdisp	56	GPIO_S (or CIF_D4)	Vcam
57	LC_R6	Vdisp	58	GPIO_R (or CIF_D5)	Vcam
59	LC_R7	Vdisp	60	GPIO_Q (or CIF_D6)	Vcam
61	LC_G2	Vdisp	62	GPIO_P (or CIF_D7)	Vcam
63	LC_G3	Vdisp	64	GPIO_O (or CIF_D8)	Vcam
65	LC_G4	Vdisp	66	GPIO_N (or CIF_D9)	Vcam
67	LC_G5	Vdisp	68	GPIO_M (or CIF_VSYNC)	Vcam
69	LC_G6	Vdisp	70	GPIO_L (or CIF_MCLK)	Vcam
71	LC_G7	Vdisp	72	GPIO_K (or CIF_PCLK)	Vcam
73	LC_B2	Vdisp	74	GPIO_J (or CIF_HSYNC)	Vcam
75	LC_B3	Vdisp	76	LC_R0	Vdisp
77	LC_B4	Vdisp	78	LC_R1	Vdisp
79	LC_B5	Vdisp	80	LC_G0	Vdisp
81	LC_B6	Vdisp	82	LC_G1	Vdisp
83	LC_B7	Vdisp	84	LC_B0	Vdisp
85	LC_EN	Vdisp	86	LC_B1	Vdisp
87	LC_VSYNC	Vdisp	88	LVDS_TX0+	LVDS

Pin number	Pin name	Power domain
89	LC_HSYNC	Vdisp
91	LC_PCLK	Vdisp
93	LVDS_TX2+	LVDS
95	LVDS_TX2-	LVDS
97	LVDS_CLK+	LVDS
99	LVDS_CLK-	LVDS
101	GND6	Vin
103	SD_CLK	VIO
105	SD_DETECT	VIO
107	SD_D1	VIO
109	SD_D3	VIO
111	GND7	Vin
113	A0	Vsysbus
115	A1	Vsysbus
117	A2	Vsysbus
119	A3	Vsysbus
121	A4	Vsysbus
123	A5	Vsysbus
125	A6	Vsysbus
127	A7	Vsysbus
129	CS_B	Vsysbus
131	CS_D	Vsysbus
133	WE	Vsysbus
135	D0	Vsysbus
137	D1	Vsysbus
139	D2	Vsysbus
141	D3	Vsysbus
143	D4	Vsysbus
145	D5	Vsysbus
147	D6	Vsysbus
149	D7	Vsysbus
151	INT_HIGHEST_PRIORITY	VIO
153	GND8	Vin
155	SPI2_CS0	VIO
157	SPI2_CLK	VIO
159	SPI2_MISO	VIO
161	SPI2_MOSI	VIO
163	GPIO_D	VIO
165	GPIO_F	VIO
167	GPIO_G	VIO
169	USB_HOST2_D+	USB
171	USB_HOST2_D-	USB
173	GPIO_H	VIO
175	GPIO_I	VIO
177	SPI1_CS0	VIO
179	SPI1_CLK	VIO
181	SPI1_MISO	VIO
183	SPI1_MOSI	VIO
185	GND9	Vin

Pin number	Pin name	Power domain
90	LVDS_TX0-	LVDS
92	LVDS_TX1+	LVDS
94	LVDS_TX1-	LVDS
96	LVDS_TX3+	LVDS
98	LVDS_TX3-	LVDS
100	GPIO_PWM	VIO
102	Vcam_OUT	Vcam
104	SD_CMD	VIO
106	SD_D0	VIO
108	SD_D2	VIO
110	Vsysbus_OUT	Vsysbus
112	A8	Vsysbus
114	A9	Vsysbus
116	A10	Vsysbus
118	A11	Vsysbus
120	A12	Vsysbus
122	A13	Vsysbus
124	A14	Vsysbus
126	A15	Vsysbus
128	CS_A	Vsysbus
130	CS_C	Vsysbus
132	CS_E	Vsysbus
134	OE	Vsysbus
136	D8	Vsysbus
138	D9	Vsysbus
140	D10	Vsysbus
142	D11	Vsysbus
144	D12	Vsysbus
146	D13	Vsysbus
148	D14	Vsysbus
150	D15	Vsysbus
152	VIO_OUT	VIO
154	GPIO_A	VIO
156	GPIO_B	VIO
158	I2C2_CLK	VIO
160	I2C2_DATA	VIO
162	GPIO_C	VIO
164	GPIO_E	VIO
166	USB_OTG_VBUS	USB
168	USB_OTG_ID	USB
170	USB_OTG_D+	USB
172	USB_OTG_D-	USB
174	USB_PWR_STAT	VIO
176	USB_PWR_EN	VIO
178	USB_HOST_D+	USB
180	USB_HOST_D-	USB
182	I2C1_CLK (HDMI_DDC_CLK)	VIO
184	I2C1_DATA (HDMI_DDC_DATA)	VIO
186	nETH1_LINK_LED	VIO

Pin number	Pin name	Power domain	Pin number	Pin name	Power domain
187	nETH2_LINK_LED	VIO	188	nETH1_SPEED_LED	VIO
189	nETH2_SPEED_LED	VIO	190	ETH1_TXD-	Ethernet
191	ETH2_TXD-	Ethernet	192	ETH1_TXD+	Ethernet
193	ETH2_TXD+	Ethernet	194	ETH_VIO_SWITCHED	VIO
195	ETH2_RXI-	Ethernet	196	ETH1_RXI-	Ethernet
197	ETH2_RXI+	Ethernet	198	ETH1_RXI+	Ethernet
199	GND10	Vin	200	VCC_BAT	Vbat

Table 33: SODIMM-200 pin assignment

6.7.2 DHCOM-X

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
1	RGMII_RXCLK	Vrgmii	2	RGMII_TXCLK	Vrgmii
3	RGMII_RXD0	Vrgmii	4	RGMII_TXD0	Vrgmii
5	RGMII_RXD1	Vrgmii	6	RGMII_TXD1	Vrgmii
7	RGMII_RXD2	Vrgmii	8	RGMII_TXD2	Vrgmii
9	RGMII_RXD3	Vrgmii	10	RGMII_TXD3	Vrgmii
11	RGMII_RX_CTL	Vrgmii	12	RGMII_TX_CTL	Vrgmii
13	RGMII_MDIO	Vrgmii	14	RGMII_MDC	Vrgmii
15	RGMII_RST	Vrgmii	16	RGMII_REFCLK	Vrgmii
17	RGMII_WOL_INT	3V3	18	RGMII_INT	3V3
19	GND	Vin	20	VCC_RGMII_OUT	Vrgmii
21	SATA_RX+	Sata	22	GND	Vin
23	SATA_RX-	Sata	24	SATA_TX+	Sata
25	GND	Vin	26	SATA_TX-	Sata
27	PCIE_RX+	PCIe	28	GND	Vin
29	PCIE_RX-	PCIe	30	PCIE_REFCLK+	PCIe
31	PCIE_TX+	PCIe	32	PCIE_REFCLK-	PCIe
33	PCIE_TX-	PCIe	34	PCIE_WAKE	3V3
35	GND	Vin	36	GND	Vin
37	CSI_CLK+	CSI	38	CSI_D0+	CSI
39	CSI_CLK-	CSI	40	CSI_D0-	CSI
41	GND	Vin	42	CSI_D1+	CSI
43	HDMI_CLK+ or DP_Lane3+	HDMI	44	CSI_D1-	CSI
45	HDMI_CLK- or DP_Lane3-	HDMI	46	GND	Vin
47	HDMI_D2+ or DP_Lane2+	HDMI	48	HDMI_D0+ or DP_Lane0+	HDMI
49	HDMI_D2- or DP_Lane2-	HDMI	50	HDMI_D0- or DP_Lane0-	HDMI
51	HDMI_CEC_IN	2V5	52	HDMI_D1+ or DP_Lane1+	HDMI
53	GND	Vin	54	HDMI_D1- or DP_Lane1-	HDMI
55	LVDS2_CLK+	LVDS	56	HDMI_HPD or DP_HPD	2V5
57	LVDS2_CLK-	LVDS	58	GND	Vin
59	LVDS2_TX2+	LVDS	60	LVDS2_TX0+	LVDS
61	LVDS2_TX2-	LVDS	62	LVDS2_TX0-	LVDS
63	LVDS2_TX3+	LVDS	64	LVDS2_TX1+	LVDS
65	LVDS2_TX3-	LVDS	66	LVDS2_TX1-	LVDS
67	GND	Vin	68	GND	Vin
69	*reserved*		70	*reserved*	
71	*reserved*		72	*reserved*	
73	*reserved*		74	*reserved*	

Pin number	Pin name	Voltage level	Pin number	Pin name	Voltage level
75	*reserved*		76	*reserved*	
77	*reserved*		78	*reserved*	
79	VCC_IN7	Vin	80	VCC_IN8	Vin

Table 34: DHCOM-X pin assignment

6.7.3 JTAG

Pin number	Pin name
1	+3V3 Output
2	GND
3	JTAG_TMS
4	#JTAG_TRST
5	JTAG_TCK
6	JTAG_TDO
7	JTAG_TDI
8	#RESET_IN
9	*Reserved*
10	*Reserved*

Table 35: JTAG interface pin assignment

7 Electrical characteristics

7.1 Power supply

Symbol	Description	Min	Typ	Max	Unit
VCC (Vin)	Power supply voltage INPUT	3.2		5.5	V
VDDA	Power supply voltage INPUT	3.2	3.3	3.4	V
V_{bat}	Battery voltage INPUT	1.3		5.5	V
V_{sysbus}	System bus voltage OUTPUT		3.3		V
$I_{Vsysbus}$	Vsysbus current			20	mA
V_{disp}	Display voltage OUTPUT		3.3		V
I_{Vdisp}	Vdisp current			20	mA
V_{cam}	Camera voltage OUTPUT		3.3		V
I_{Vcam}	Vcam current			20	mA
V_{IO}	I/O voltage OUTPUT		3.3		V
I_{VIO}	VIO current			20	mA
$V_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED voltage OUTPUT		3.3		V
$I_{ETH\_VIO\_SWITCHED}$	ETH_VIO_SWITCHED current			60	mA
VIH_3V3	Digital input high voltage	2.0	3.3		V
VIL_3V3	Digital input low voltage		0	0.8	V

Table 36: DC operating conditions

8 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Operating temperature range	-40		85	°C

Table 37: Temperature Range

9 Appendix