DHCOM DESIGN GUIDE

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IDEA TECHNOLOGY SOLUTION

History

Version	Date	Description or changes	Name
V1.0	2012-09-19	First issue	AG
V1.1	2012-10-04	English language translation	AG
V1.2	2013-04-11	- Add ethernet port 2 to unconnected pin description - Add VCC_BAT, VDDA_Audio and VSSA_Audio to unconnected pin description. - Add i.MX25 special note for alternative GPIO pins (see 3.7). - Add DHCOM SPI2 design note (see 3.5). - Add 15k resistors to USB schematics (see 3.10). - Add note for RGB interface unconnected pins (see 2.2). - Add note for power supply limits (see 4.0). - Add backlight enable GPIO information (see 3.6 and 3.7). - Add HSYNC and VSYNC lines to 8bit LVDS example Figure 9. - Add 6bit LVDS example (see 3.6.2)	AG
V1.3	2014-02-11	- Add UART2 design note (see 3.4) - Add SPI1 design note (see 3.5) - Add i.MX25 GPIOs to "What requires attention" (see 2.3) - GPIO Level Shifter information moved from chapter 3.7 to 2.3	AG
V1.4	2014-07-02	- Add voltage information for i.MX6 and AM335x to table 3	AG
R01	2016-09-23	- SPI multi master design note (see 3.6) - Add power button chapter (see 3.2) - Add DHCOM-X unconnected pins information (see table 2) - Add UART RS-485 design note (see 3.5) - Changed VBUS buffer size for USB host interface (see figure 24) - Changed VBUS buffer size for USB OTG interface (see figure 21 and 22) - Add cooling solution instructions (see 4) - Add core module fixation instructions (see 5) - Add mainboard placement drawing (see 6) - Add USB OTG reverse current protection (see 3.11.3) - Add high speed connector schematic (see 9.2) - Gbit ethernet connection (see 3.13) - Add Reset_in and reset_out unconnected pin information (see 3.4 and 2.2) - Add 3,3V power supply recommendation (see 3.1) - Add digital audio interface (I2S) description (see 3.3.1) - Add note to technical modifications and responsibility (see 1) - Add note to use GPIO_G as backlight enable pin (see 3.7) - Delete max. trace length information at lvds layout guidelines - Add USB_OTG_VBUS voltage information (see 7.) - Add power supply layout guidelines (see 3.1) - Add FTDI USB-to-UART connection design note (see 3.5) - Moved "i.MX25 GPIOs" chapter from 2. to 3.8 - Changed LC_* unconnected pin recommendation (see 2.2) - Add Connector information (see 10.) - Changed USB VBUS input capacitor connection from GND to earth (Figure 21, 22, 23 and 24)	AG
R02	2016-09-27	- Add chapter 4.5 "Test conditions" - Add some information's to cooling examples (see 4.3 and 4.4)	AG
R03	2018-02-22	- Add figure 47 "Graphite foil to mounting plate connection" - Add figure 11 "FTDI connection example" - Add ESD protection diodes to audio I2S interface example figure 3 - Add connector pin numbers to figure 50 - Add dual channel LVDS pixel mapping (see 3.7.3) - Add chapter 3.14 PCIe - Add new core modules to table 8 and table 12 - Add chapter 3.7.4 HDMI - Add chapter 5.3 Carrier Board Space Requirements - Add Android button information to chapter 3.8.1 - Add Touch interrupt line information to chapter 3.8.1 - Changed Vbat conditions (see 3.2) - Add max. trace length to Ethernet Layout guidelines	AG

R04	2018-06-28	-	Add Ethernet layout note regarding 49.9 ohm pull-up resistors on the differential lines. (see 3.13)	AG
		-	Adjust Ethernet Layout GND planes at figure 30	

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1 Introduction

This document serves as a guide for the design of a DHCOM mainboard. It includes example circuits for external connected components to a DHCOM module. Also included in this document are layout rules.

Note: Subject to technical modifications; no responsibility is accepted for the accuracy of this information.

2 What requires attention?

2.1 Compatibility of the DHCOM platform

The DHCOM standard defines functions (such as USB, I2C, SPI, ...) that are available at the predefined position on the SODIMM-200 connector. The pin assignment for the 200 pins is also defined and identical for all DHCOM core modules.

The DHCOM specification describes functional groups to ensure the compatibility between different DHCOM modules. Each functional group has its own supply voltage, which is made available on the SODIMM-200 connector via a voltage level output (Vcam_OUT, Vdisp_OUT, Vsysbus_OUT and VIO_OUT). Level shifters on the customer-specific mainboard establish the compatibility between different DHCOM modules. These level shifters can also (e.g. for reasons of cost) be removed from the customer design. In this case, however, the customer loses the compatibility with the DHCOM standard.

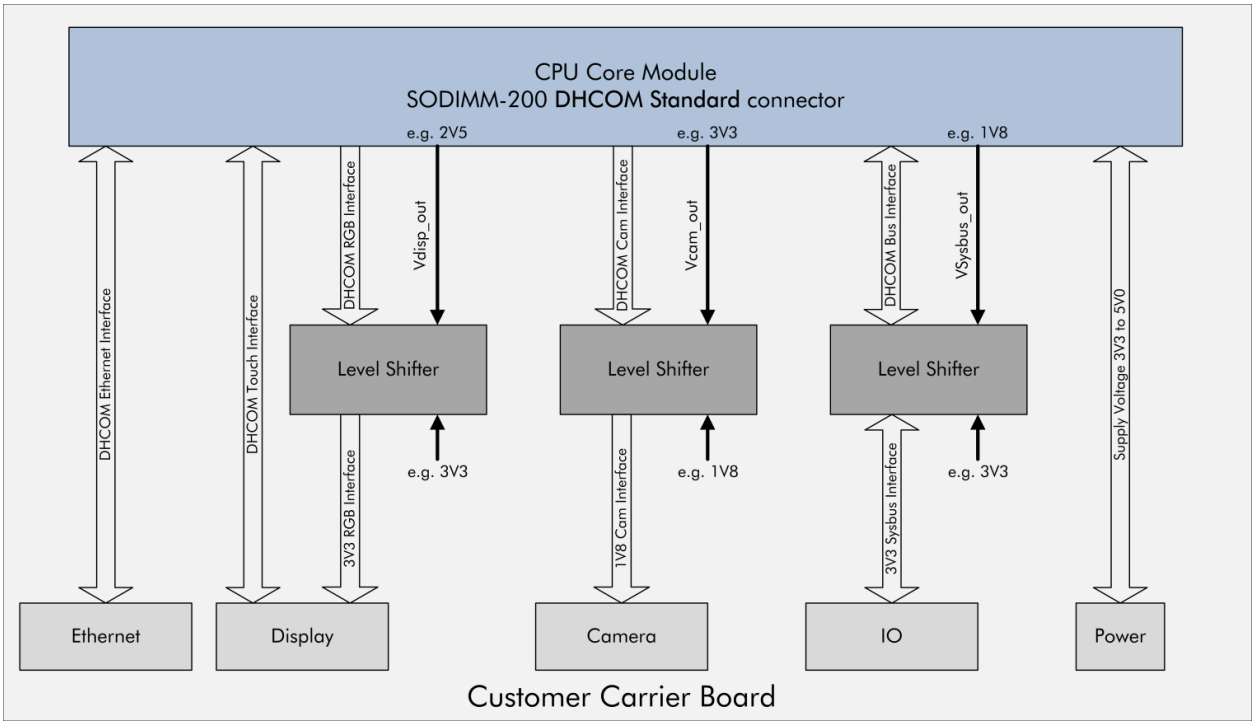


Figure 1: DHCOM functional groups concept

Important:

With the level shifter concept it is possible to support all core modules developed by DH electronics in the future. If you only wish to use the current DHCOM modules (DHCOM i.MX25, AM35x, i.MX6 and AM335x) you only need to use level shifters in special cases, see Table 12: Voltage groups on page 49.

Summary:

At the moment you only need level shifters at the address and data bus interface, if you wish to use parallel a address and data bus, i.MX25 and another DHCOM core module in the same mainboard hardware.

2.2 Unconnected pins

The following SODIMM-200 pins must be terminated if they are not used:

Pin name	Description	SODIMM pin number	Terminating resistance or voltage
VCC_BAT	Core Module Battery voltage input	200	3.3V or 5V
VDDA_Audio	Audio Codec supply voltage input	10	3.3V
VSSA_Audio	Audio Codec Ground	9	GND
RESET_IN	**System Reset input (active low)**	**21**	**PU + 100nF capacitor**
RESET_OUT	**System Reset output (active low)**	**20**	**PU + 100nF capacitor**
TSPX	Resistive Touch: 4 wire (X +)	12	PD
TSMX	Resistive Touch: 4 wire (X -)	14	PD
TSMY	Resistive Touch: 4 wire (Y -)	16	PD
TSPY	Resistive Touch: 4 wire (Y +)	18	PD
AD0	Analog input 0	8	PD
AD1	Analog input 1	6	PD
AD2	Analog input 2	4	PD
AD3	Analog input 3	2	PD
nETH1_LINK_LED	Port 1: Activity LED connection	186	PD
nETH1_SPEED_LED	Port 1: Speed LED connection	188	PU
ETH1_TXD-	Port 1: Ethernet TX Differential Output (minus)	190	PD
ETH1_TXD+	Port 1: Ethernet TX Differential Output (plus)	192	PD
ETH1_RXI-	Port 1: Ethernet RX Differential Input (minus)	196	PD
ETH1_RXI+	Port 1: Ethernet RX Differential Input (plus)	198	PD
nETH2_LINK_LED	Port 2: Activity LED connection	187	PD
nETH2_SPEED_LED	Port 2: Speed LED connection	189	PU
ETH2_TXD-	Port 2: Ethernet TX Differential Output (minus)	191	PD
ETH2_TXD+	Port 2: Ethernet TX Differential Output (plus)	193	PD
ETH2_RXI-	Port 2: Ethernet RX Differential Input (minus)	195	PD
ETH2_RXI+	Port 2: Ethernet RX Differential Input (plus)	197	PD
USB_OTG_VBUS	OTG Client: VBUS Input line OTG Host: USB bus supply voltage	166	PD
USB_OTG_D+	USB OTG differential Signal positive line	170	PD
USB_OTG_D-	USB OTG differential Signal negative line	172	PD
USB_HOST_D1+	USB Host differential Signal positive line	178	PD
USB_HOST_D1-	USB Host differential Signal negative line	180	PD
USB_HOST_D2+	USB Host differential Signal positive line	169	PD
USB_HOST_D2-	USB Host differential Signal negative line	171	PD
MIC_IN or I2S_RXFS	Microphone Input Signal or Receive Frame	1	PD

Pin name	Description	SODIMM pin number	Terminating resistance or voltage
	sync signal		
LINEIN_L or I2S_RXD	Line-In Left or Data receive signal	5	PD
LINEIN_R or I2S_RXC	Line-In Right or Receive clock signal	7	PD
SD_DETECT	SD/SDIO/MMC card detection(active high)	105	PD
INT_HIGHEST_PRIORITY	Highest priority interrupt pin (active low)	151	PU
~~LC_*~~ [1]	~~RGB display interface lines~~ ~~Note: Regarding EMC it is recommended to terminate RGB interface lines.~~	~~49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 89, 91~~	~~PD~~

Table 1: Unconnected SODIMM-200 Pins

[1] Do not use Pull-down resistors on the LC_* lines if unconnected, because AM335x use these pins as boot mode pins.

The following DHCOM-X connector pins must be terminated if they are not used and connector is available:

Pin name	Description	SODIMM pin number	Terminating resistance or voltage
RGMII_INT	PHY interrupt (active low)	18	PU
RGMII_WOL_INT	PHY Wake-on-LAN interrupt (active low)	17	PU
PCIE_WAKE	PCIe wake signal (active low)	34	PU

Table 2: Unconnected DHCOM-X Pins

PD = Pull-down resistor to GND; PU = Pull-up resistor to 3V3

Note: For Pull-up or Pull-down resistors, a value of 10kohm is recommended unless otherwise stated.

3 Interface

The chapters that follow give design examples for the interfaces on the SODIMM-200 connector and prescribe design rules for a customer specific mainboard design.

3.1 Power supply

The DHCOM modules have the following voltage inputs:

- Vin = core module supply voltage
- Vbat = battery voltage

Note: DH electronics recommends 3.3V for core module power supply to decrease the power consumption of the whole system.

Regarding the current consumption from the Vin supply, please refer to the user manual of the core module.

Layout routing guidelines:

It is necessary to connect the power supply to the SODIMM-200 connector with low trace impedance. Be careful of adding via's to the power supply connection.

3.2 VBAT

If no buffering of the battery voltage is provided on Vbat, this pin must be connected to Vin. Otherwise, see the following example of a Gold Cap connection:

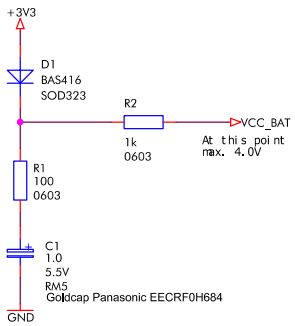


Figure 2: Vbat connection example

Note: At older user manuals and design guide versions, Vbat was stated with 3.3V up to 5.5V. Please ensure that Vbat pin is sourced with a maximum voltage of 4.0V at the SODIMM pin. Otherwise the I2C communication between RTC and CPU doesn't work anymore.

3.3 Power Button

The DHCOM standard doesn't provide a power button input.

Explanation: We don't support power button input because of one simple problem. If we have such an input we could only power off the core module power with it. The mainboard voltage would remain at on state. This has the consequence that all interfaces of the core module will be powered from the mainboard side and furthermore undefined things happen.

Workaround: If a power button for complete system power On/Off is needed, we recommend using a power button On/Off controller on the mainboard. Maybe the Linear Technology LTC2953 would be a good choice (http://www.linear.com/product/LTC2953).

3.4 Audio interface

Depending on the specific core module the audio interface on the SODIMM-200 connector is analog (OnModule audio codec) or digital (I2S interface). The following table shows the audio interfaces of the specific core modules:

DHCOM module	Analog Interface (On board audio codec)	Digital I2S interface
i.MX25	-	On request
AM35x	Yes (TI TLV320AIC23B)	-
AM335x	-	Yes
i.MX6	-	Yes

Table 3: Core module audio interfaces

The pins on the SODIMM-200 connector are shared between analog and digital interface:

SODIMM pin number	SODIMM pin name	Description	IO Type	SODIMM pin name	Description	IO Type
	Analog Interface			**Digital I2S interface**		
10	VDDA_Audio	Audio Codec supply voltage input	PWR_I	VDDA_Audio	Audio Codec supply voltage input	PWR_I
9	VSSA_Audio	Audio Codec Ground	PWR_I	VSSA_Audio	Audio Codec Ground	PWR_I
1	MIC_IN	Microphone Input Signal	I	*I2S_RXFS**	*Receive Frame sync signal*	/
3	MIC_GND	Microphone Ground	PWR_I	-	-	-
5	LINEIN_L	Line-In Left	I	I2S_RXD	Data receive signal	I
7	LINEIN_R	Line-In Right	I	*I2S_RXC**	*Receive clock signal*	/
11	HP_GND	Headphone Ground	PWR_O	I2S_TXFS	Transmit Frame sync signal	O
13	HP_OUT_LEFT	Headphone Output left	O	I2S_TXC	Transmit clock signal	O
15	HP_OUT_RIGHT	Headphone Output right	O	I2S_TXD	Data transmit signal	O

Table 4: Audio interface pins

** The signals are not connected to the core modules AM335x and i.MX6.*

3.4.1 Digital

The I2S interface of the current DHCOM core modules (AM335x and i.MX6) supports only DHCOM (master) to Audio Codec (slave) mode with the available I2S interface on the SODIMM-200 connector. Otherwise the signals I2S_RXFS and I2S_RXC would be needed.

The following figure shows an example how to connect an audio codec to the digital DHCOM audio interface.

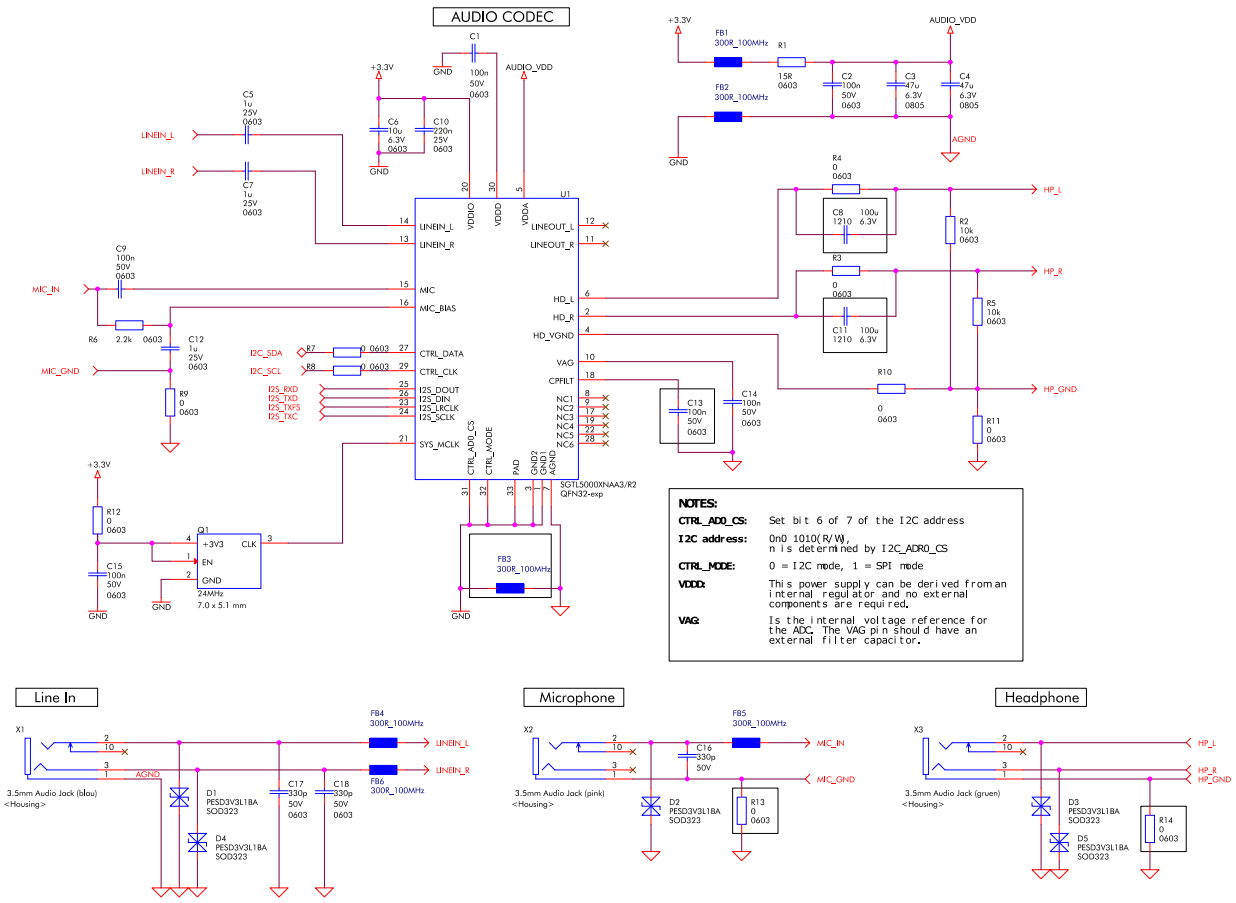


Figure 3: Audio codec connection

3.4.2 Analog

Analog power supply:

For the analog audio part of DHCOM modules, separate supply inputs are available on the SODIMM-200 connector:

- VDDA_Audio
- VSSA_Audio

These must be supplied from a separately filtered supply voltage. An example of such a filter is shown in the next figure:

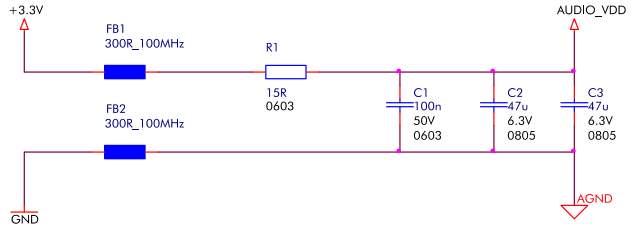


Figure 4: Audio supply voltage filter

Note: The design of the filter depends largely on the quality of the supply voltage, the filter shown can therefore only be regarded as an example.

Microphone:

MIC_IN is a high-impedance, low-capacitance input that is supplied with a reference voltage by the audio CODEC. The internal circuit is suitable for an electret microphone. The maximum output current is about 3 mA. An example for the connection of a jack socket is shown in the next figure:

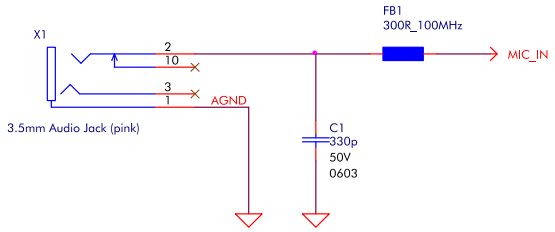


Figure 5: Audio microphone connection

Line In:

The DHCOM audio CODEC has a line input for left and right audio channels. A voltage divider on the core module halves the input signal. This reduces the 2 x V_{RMS} of a CD player signal to the nominal 1 x V_{RMS} input to the audio CODEC. An example for the connection of a jack socket is shown in the next figure:

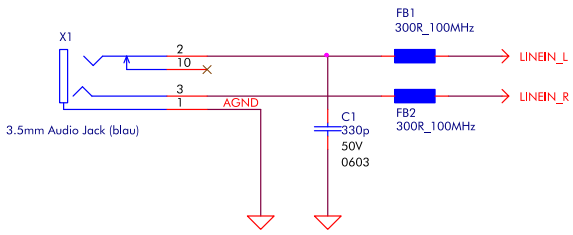


Figure 6: Audio line in connection

Headphone:

The DHCOM audio CODEC has a headphone output for left and right audio channels. The output is designed to drive 16R and 32R headphones. The DC decoupling is on the core module so that no coupling capacitors are required on the mainboard. An example for the connection of a jack socket is shown in the next figure:

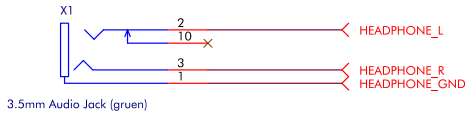


Figure 7: Audio headphone connection

Layout routing guidelines:

For all analog audio signals, particular attention must be given to the connecting lines. These should be routed as far as possible from digital signals. It should also be ensured that separate ground areas are placed beneath the analog audio signals and connected to audio ground.

3.5 Reset & Interrupt

The DHCOM modules have a RESET_IN and a RESET_OUT. Both signals are "active low". If the RESET_IN is connected to a push-button, it must be de-bounced and extended (min. 1.5 ms) as shown in the example connection:

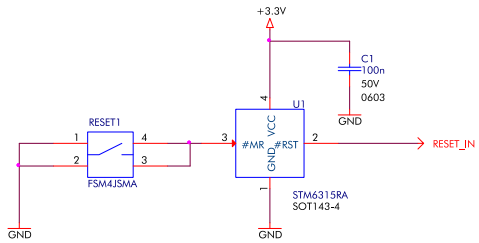


Figure 8: Reset switch

The RESET_OUT signal is pulled "low" if the core module is in the Reset state. It can be used on the mainboard as reset line.

Note: Because of better EMI performance it is recommended to connect a 10k pull-up resistor and 100nF capacitor to GND to the reset_in as well as reset_out pins. Don't leave these pins unconnected.

3.6 UART

The DHCOM modules have up to 3 UART interfaces, however, only UART_1 is connected as a "fully functional UART".

Note: It is necessary to provide a connection to the DHCOM UART1, as the core module bootloader could be controlled via the UART1. A minimum connection level should be provided via solder pads.

As an example, the following diagram shows a circuit for the connection of an RS-232 transceiver:

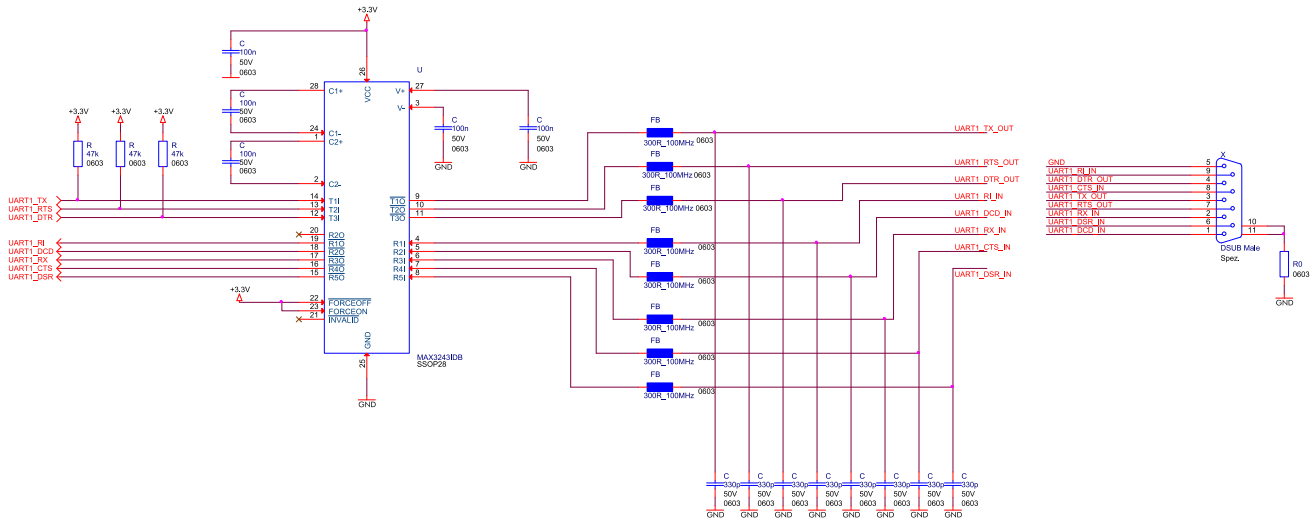


Figure 9: FF UART RS-232 Transceiver

RS-485 Design note:

Because of software implementation it is recommended to use the following pins as TX and RX enable of RS-485 interfaces.

DHCOM UART	RS-485 pin description	SODIMM pin number	DHCOM pin description
UART1	TX enable	Not yet defined.	
	RX enable		
UART2	TX enable	68	GPIO_M
	RX enable	66	GPIO_N
UART3	TX enable	64	GPIO_O
	RX enable	62	GPIO_P

Table 5: Unconnected DHCOM-X Pins

Design notes:

Special attention must be paid with FTDI USB-to-UART cable connection to the DHCOM UART's. If the DHCOM device is no longer powered and the USB side is still connected to a Host PC, the Tx signal continues sourcing power to the computer on module. After restart problems may occur on the DHCOM system, because of reverse current (we noticed problems with eMMC or SD card connection).

Therefore, the connection should be disconnected or isolated if the power supply of the DHCOM system is switched off.

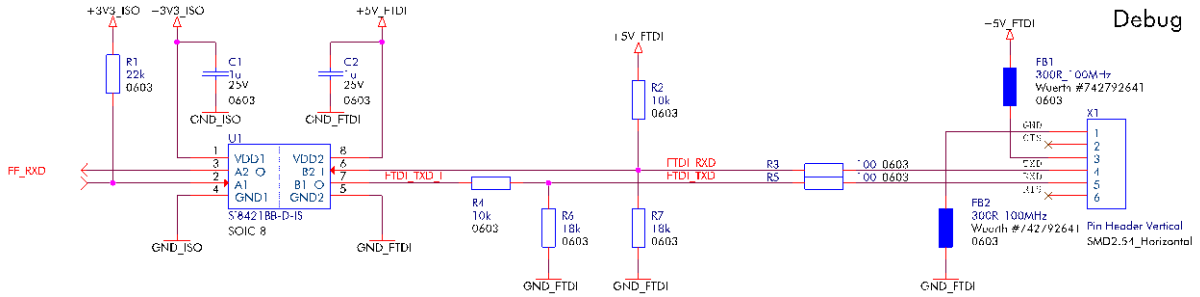


Figure 10: FTDI isolated connection example

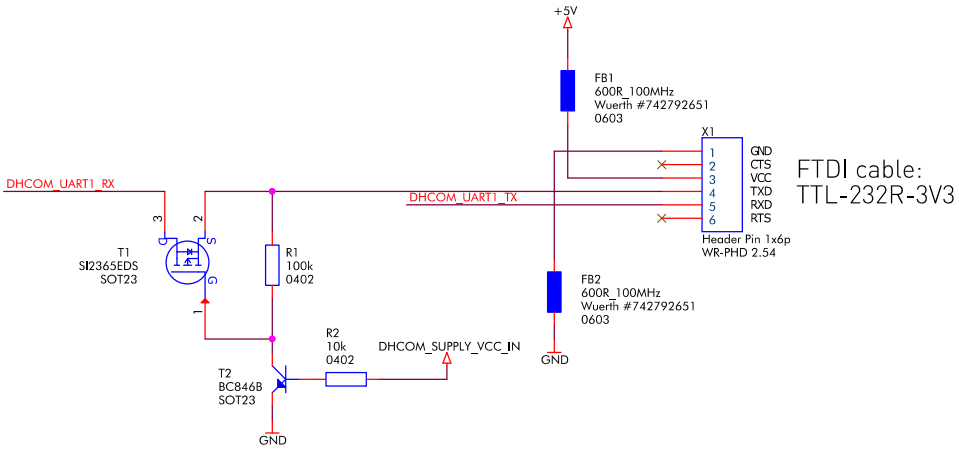


Figure 11: FTDI connection example

Design note for DHCM-iMX25-01D2:

The DHCOM UART2 hardware flow control pins (CTS, RTS) are only implemented with i.MX25 gpio pins. The CTS gpio is also used on the core module for boot mode configuration. In addition to that the mainboard design must ensure that this pin is not driven at power up.

3.7 SPI

Design notes:

- Some DHCOM core modules boot up from OnBoard SPI Flash. This SPI interface is also available outside of the module via DHCOM SPI1 interface with another chip select. In addition to that the mainboard design must ensure that these pins are not driven at power up. If level shifters are used, the DHCOM SPI1 interface needs to be connected to a separate level shifter. The enable pin of the level shifter needs to be activated with the DHCOM SPI1 chip select.
- SPI with external Master:
  In this case the mainboard design must ensure, that the DHCOM SPI1 lines (MISO, MOSI and CLK) are not driven from the external Master at boot up, otherwise the DHCOM module doesn't boot because the MISO, MOSI and CLK lines are shared with the DHCOM boot flash.

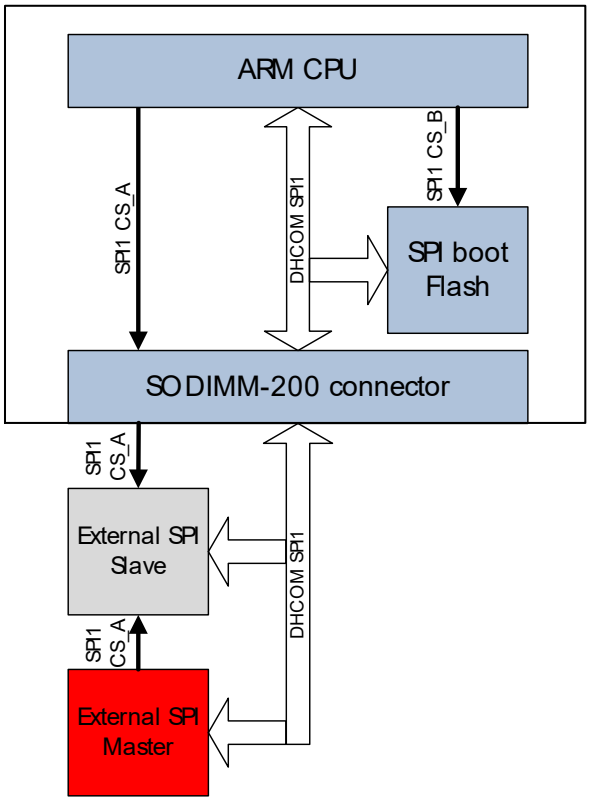


Figure 12: SPI multi master system

Design note for DHCM-iMX25-01D2:

The DHCOM SPI2 interface pins are shared with some DHCOM camera interface pins. Therefore it is only possible to use the pins either for the camera interface or for SPI2.

3.8 Display interface

The DHCOM standard offers 24-bit RGB signals and 4 LVDS pairs (+ 1x clock pair) as display interface. Unlike the RGB Interface, which is always available with at least a 16-bit data bus width, LVDS is not available as standard from some DHCOM modules. An example of an RGB-LVDS converter is therefore given in chapter 3.8.2 LVDS interface.

Note: It is possible to use the DHCOM GPIO_A – GPIO_I pins as backlight enable GPIO. It is recommended to use GPIO_G as backlight enable pin, because of software compatibility. The additional GPIOs GPIO_J – GPIO_W do not support the backlight enable functionality.

3.8.1 RGB interface

Displays with a wide range of colour formats (RGB 565, RGB 666, RGB 888, etc.) can be connected to the parallel RGB interface. If not all 24 data lines are required, it must be ensured that it is the most significant bits that are connected.

Layout routing guidelines:

It is recommended that the RGB interface lines are routed with equal lengths and spaced as far as possible from other signals. The max. RGB line length between the SODIMM-200 connector and the display connector is 150 mm. Furthermore, unused display lines must be terminated with an appropriate resistance to reduce interference (maintain EMC).

3.8.2 LVDS interface

If no LVDS interface is available from the DHCOM module, the circuit in the following figure (TI SN65LVDS93A LVDS transmitter) can be used for reference.

Note: Be careful with the LVDS data mapping. Your display may use different data mapping.

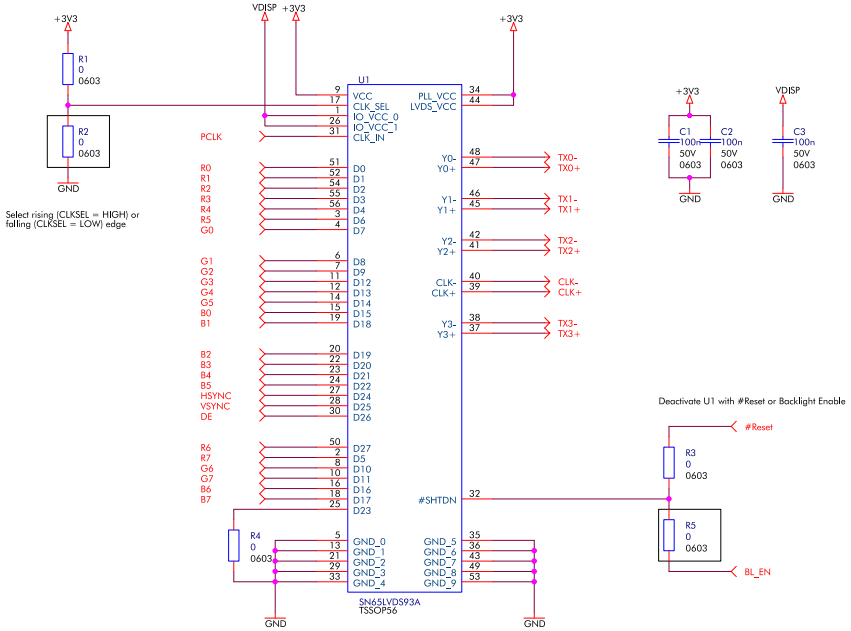


Figure 13: 8bit LVDS (16.7M colors) Circuit Example

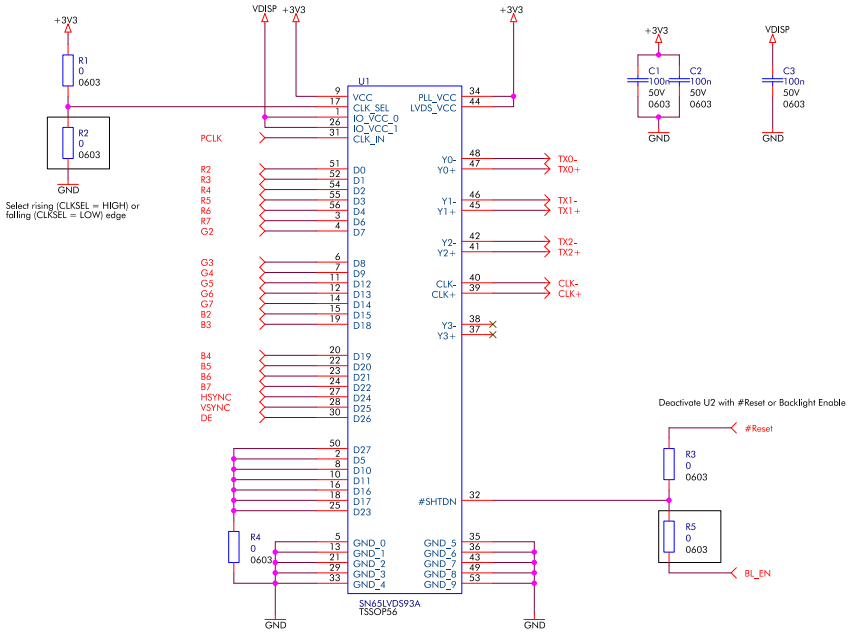


Figure 14: 6bit LVDS (262k colors) Circuit Example

Layout routing guidelines:

The given layout notes belong to the LVDS clock and data lines. In addition, conductor lengths within an LVDS channel must be equalised with a maximum difference between the differential pairs of 0.25 mm.

- Differential Impedance: 100Ω ±20%
- Pair-to-pair pitch: min. 0,8mm
- Maximum via count: 2
- „Differential pairs" must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.

3.8.3 Dual channel LVDS

If the DHCOM LVDS interface is connected to dual channel LVDS display, the following pixel mapping must be used:

- DHCOM LVDS 1 (SODIMM-200) = odd pixels
- DHCOM LVDS 2 (DHCOM-X high speed connector) = even pixels

3.8.4 HDMI

The DHCOM standard offers one HDMI interface on the high speed connector (DHCOM-X interface). Please be aware that HDMI have licencing restrictions in place. The following figure shows an example of a HDMI connection:

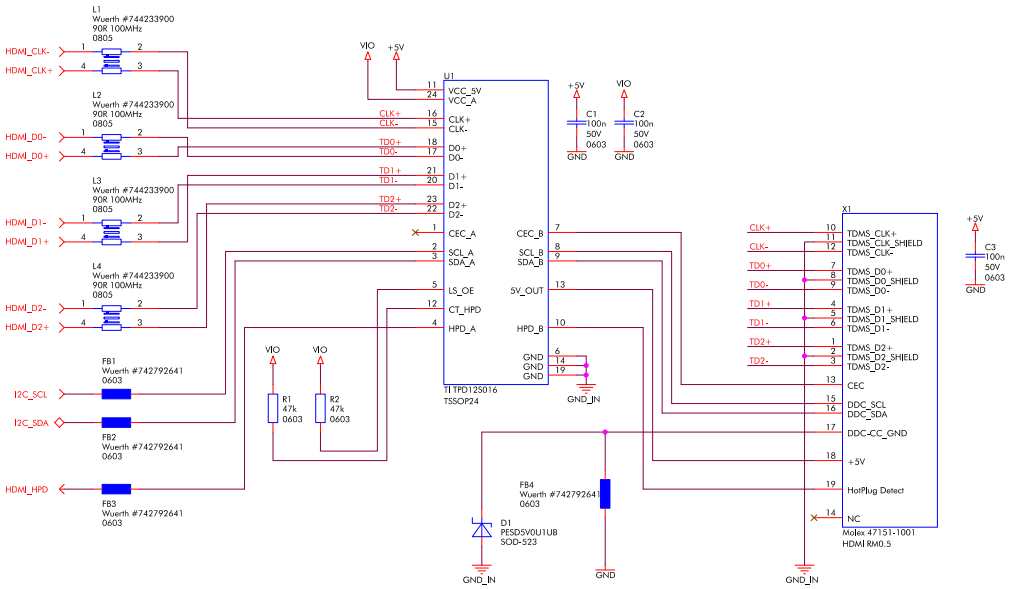


Figure 15: HDMI example

HDMI Layout routing guidelines:

- Max. frequency: HDMI 1.4a: 1.65GHz (340 MHz pixel clock)
- Differential Impedance: 100Ω ±15%
- Single ended impedance: 50Ω ±15%
- Trace lengths equalised within the diff. pairs: 1mm
- Trace length difference within a pair: 0.125mm
- no stub lines
- Maximum trace length from DHCOM connector to HDMI connector: 200mm
- Spacing to other signals (especially clock signals): min. 1.5mm
- Pair-to-pair pitch: min. 0,5mm
- Maximum via count: 2
- „Differential pairs" must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.

3.9 GPIO

3.9.1 GPIO_A – GPIO_I

The DHCOM standard offers a maximum of 9 primary function GPIO pins.

Notes:

- It is possible to use the DHCOM GPIO_A – GPIO_I pins as backlight enable GPIO. The additional GPIOs GPIO_J – GPIO_W do not support the backlight enable functionality.
- **Android buttons:**
  With the DHCOM standard Android Images the following GPIOs are connected to active low buttons, for the following Android functionality:
  - GPIO_A: Volume up button
  - GPIO_B: Back button
  - GPIO_C: Power button
  - GPIO_D: Volume down and recovery button

  If the buttons functionality is not needed with Android standard images, the GPIOs must be set to high via a pull-up.
- **Default Touch Interrupt pin:**
  In combination with capacitive Touch controllers the following GPIOs are used by default (see Linux device tree) as touch interrupt lines:
  - GPIO_E: At PDK2 display adapter boards

- GPIO_H: At picoITX2 display adapter boards

- **DHCM-iMX25-01D2 GPIOs:**

  If an i.MX25 GPIO_A – GPIO_H is used as output, an additional driver is required on the mainboard side. If the pin is used as input a buffer should be provided on mainboard hardware.

  Background: On the DHCM-iMX25-01D2 module, additional level shifters (Texas Instruments TXS0108E) are used for the GPIO signals, which raise the GPIO signal level to 3.3 V (Figure 16). Because of their architecture (automatic direction recognition), these can only deliver a drive current of <100 µA (highly load-dependent). For this reason it is recommended that GPIO signals that are used as output are provided with an additional driver circuit (e.g. SN74AHC1G125) or a transistor stage on the mainboard (Figure 17). In the case of input usage, a buffer on the mainboard hardware side is recommended (Figure 18) to protect the Level Shifter direction detection.

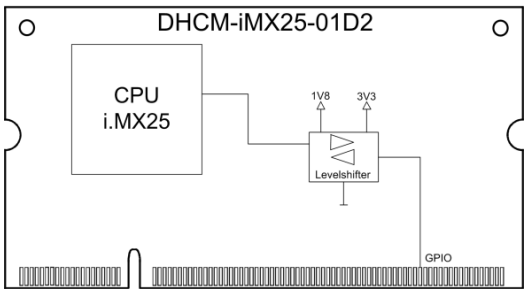


Figure 16: GPIO circuit on DHCM-iMX25-01D2

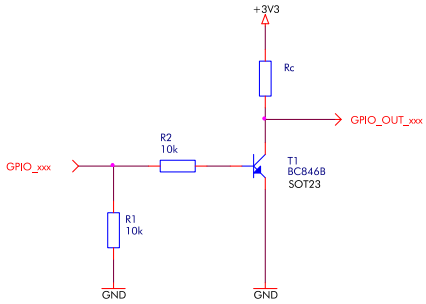


Figure 17: GPIO circuit as output

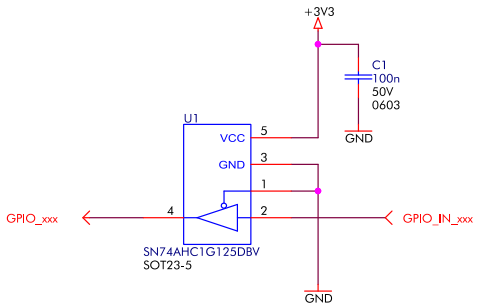


Figure 18: GPIO circuit as input

3.9.2 GPIO_J – GPIO_W (alternative GPIOs)

If the GPIOs (GPIO_A – GPIO_I) are not sufficient, the camera interface pins can also be used as GPIOs. This increases the number of available GPIOs from 9 to a maximum of 23. The maximum number depends on whether the camera interface is available on the core module in question and on how many data lines are available.

Camera interface pin	Alternative DHCOM GPIO name	SODIMM pin number
CIF_HSYNC	GPIO_J	74
CIF_PCLK	GPIO_K	72
CIF_MCLK	GPIO_L	70
CIF_VSYNC	GPIO_M	68
CIF_D9	GPIO_N	66
CIF_D8	GPIO_O	64
CIF_D7	GPIO_P	62
CIF_D6	GPIO_Q	60
CIF_D5	GPIO_R	58
CIF_D4	GPIO_S	56
CIF_D3	GPIO_T	54
CIF_D2	GPIO_U	52
CIF_D1	GPIO_V	50
CIF_D0	GPIO_W	48
Vcam_OUT	Reference Voltage for GPIO_J – GPIO_W	102

Table 6: Alternative GPIOs

Important:

- For these GPIOs, Vcam_OUT is reference voltage instead of VIO_OUT.
- **DHCM-iMX25-01D2**: The camera interface pins CIF_D2, CIF_D3, CIF_D4 and CIF_D6 are shared with DHCOM SPI2 interface. Therefore it is only possible to use the pins either for the camera interface, for SPI2 or for GPIO.

3.10 SDIO

Depending on the DHCOM module the SDIO interface can be used parallel or alternative to the OnBoard microSD slot, where alternative means that it is possible to switch between the slots during operation.

Core module examples:

- DHCM-iMX25-01D2 → DHCOM SDIO interface can be used as an alternative to the microSD slot.
- DHCM-AM35-01D2 → DHCOM SDIO interface can be used in parallel with the microSD slot.

An SD slot example circuit is shown in the next figure:

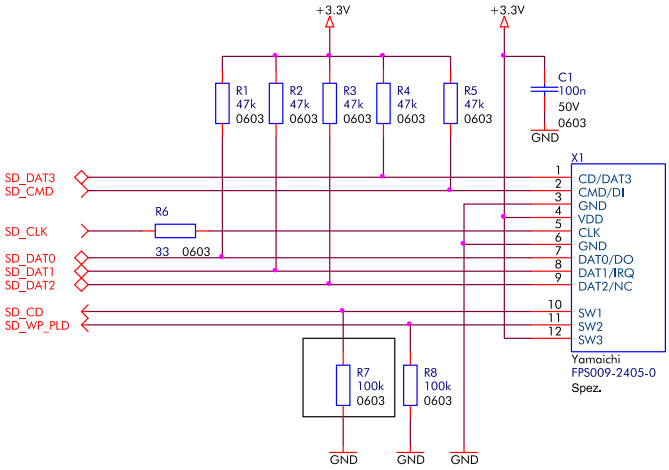


Figure 19: SD card connection

Layout routing guidelines:

The max. SDIO interface line length from the SODIMM-200 connector without additional bus driver is 80 mm. All lines should be routed with matched trace length. In addition, a 33R resistor should be inserted into the clock line, as close as possible to the SODIMM-200 connector. For line lengths near 80 mm, it is also a good idea to include a buffer in the clock line:

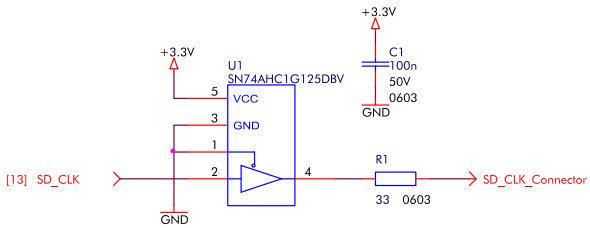


Figure 20: SD Clock buffer circuit

3.11 System bus

The DHCOM modules support the connection of peripherals by a parallel address and data bus. The memory bus interface supports 16 data bits, 16 address bits and a maximum of 5 chip select lines (see DHCOM Specification).

The address lines address wordwise (16-bit) and can address a maximum of 128 kByte.

3.11.1 8-bit access

There is no special 8-bit mode. If an 8-bit device is connected, access internal to the CPU is still to word addresses. The high Byte of the data is ignored. If, for example, address 0x1 should be read on an 8-bit device then address 0x2 must be used CPU internal.

Word (16bit) Adresse	DHCOM Adressbits [A15...A0]	Daten [D15...D0]							
0x0000	...0000b								
0x0002	...0001b								
0x0004	...0010b								
...									

Figure 21: System bus 8-bit access

3.11.2 16-bit access

The connection of a Davicom Ethernet controller is shown in the next figure:

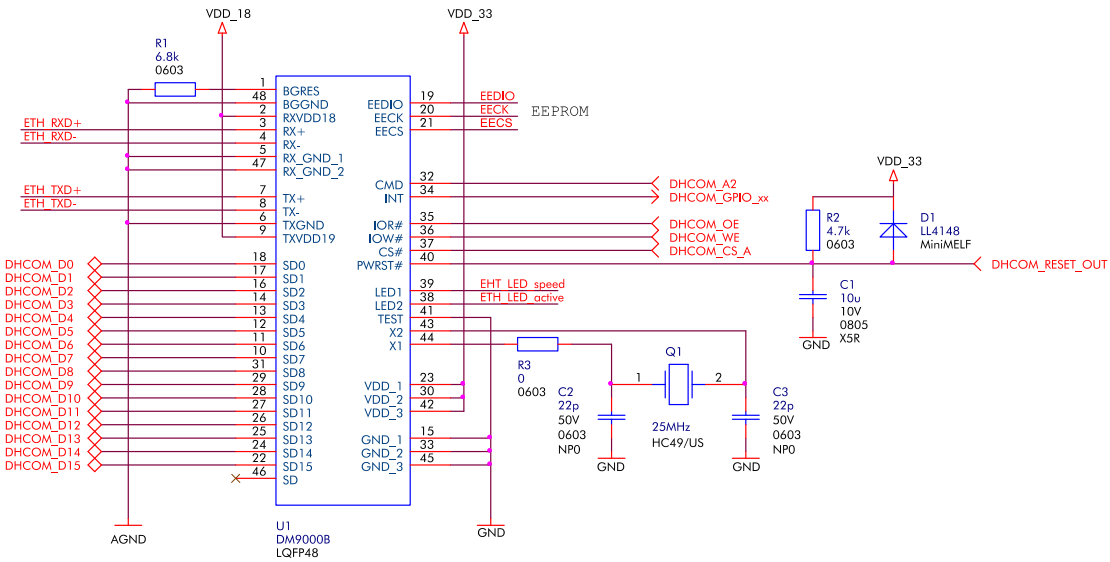


Figure 22: System bus 16-bit Davicom Ethernet example

In the case of the Davicom DM9000, the CMD input is controlled via address A2. The address 0x8 must be used to set the CMD input to 1.

3.12 USB

A DHCOM core module has at least one USB host and one USB OTG interface. If an interface is a USB 2.0 High Speed interface, it will also support USB 1.1.

Layout routing guidelines:

The USB data lines are to be routed as differential pairs with lengths equalised to within 0.25 mm. Furthermore, no stub lines may be connected to the data lines.

- Differential impedance: 90Ω ±15%
- Pair-to-pair pitch: min. 0,9mm
- Spacing to CLK signals: min. 1,5mm
- Maximum trace length from DHCOM connector to EMI choke: 200mm
- Maximum trace length from EMI choke to ESD diode: 12,0mm
- Maximum trace length from ESD diode to connector: 5,0mm
- Maximum via count: 2
- „Differential pairs“ must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.

3.12.1 USB OTG interface

The DHCOM USB OTG port has no USB Power Enable or USB Overcurrent pins. In the host case, the VBUS is switched on with the ID Pin (ID = Low → Host / ID = Floating → Client) and the Overcurrent output of the USB power management unit can, if desired, connected to a DHCOM GPIO. This leaves the possibility open to the customer to monitor the Overcurrent status in an application.

The following figure shows an example of a USB OTG connection:

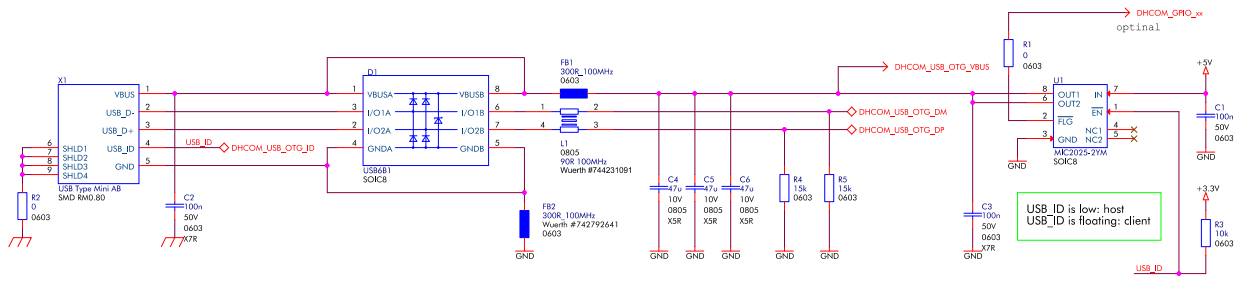


Figure 23: USB OTG connection

USB OTG as host-only interface:

The following figure shows the use of the USB OTG port as a host-only interface:

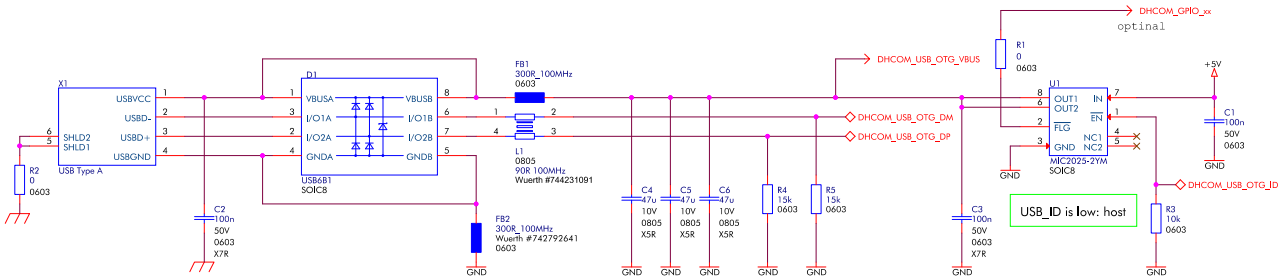


Figure 24: USB OTG host connection

USB OTG as client-only interface:

The following figure shows the use of the USB OTG port as a client-only interface:

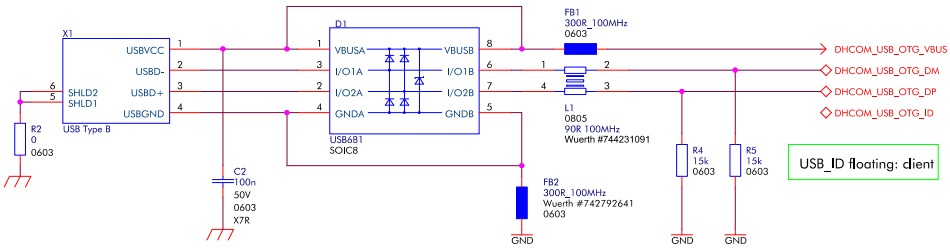


Figure 25: USB OTG client connection

3.12.2 USB host interface

The two DHCOM USB host interfaces share the two signals USB_PWR_EN and USB_PWR_STAT, i.e. the VBUS voltages can only be switched on and off together. The following figure shows an example of a USB host connection:

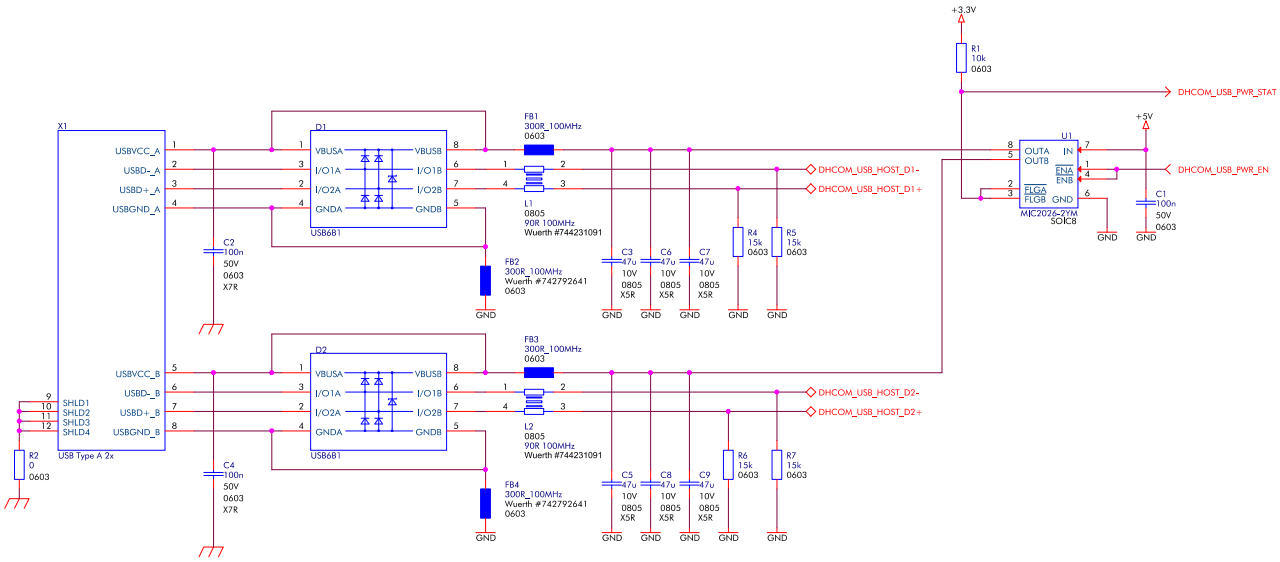


Figure 26: USB host connection

3.12.3 USB OTG reverse current protection

With USB OTG the possibility of device reverse powering exists if the B device (e.g. DHCOM USB OTG port) is not powered up anymore and the A device (e.g. PC USB host port) continues to source power.

This problem can be fixed with special reverse current protection USB power devices like the TI TPS25940 or with special circuits like that shown in the next figure:

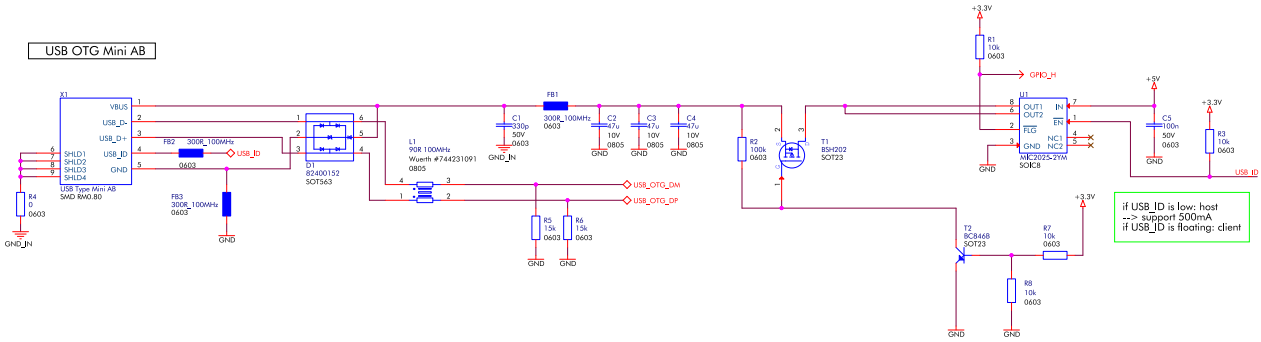


Figure 27: USB OTG reverse current protection

Note: The transistors T1 and T2 ensure that voltage is only applied to the DHCOM mainboard via USB path, if the module is also supplied with power (+3.3V is active on DHCOM mainboard).

3.13 Ethernet interface

A special feature of the DHCOM Ethernet interface is the voltage ETH_VIO_SWITCHED. Using this voltage, the Ethernet transmitter can be disabled in low power mode to save power.

The following figure shows an example of an Ethernet connection:

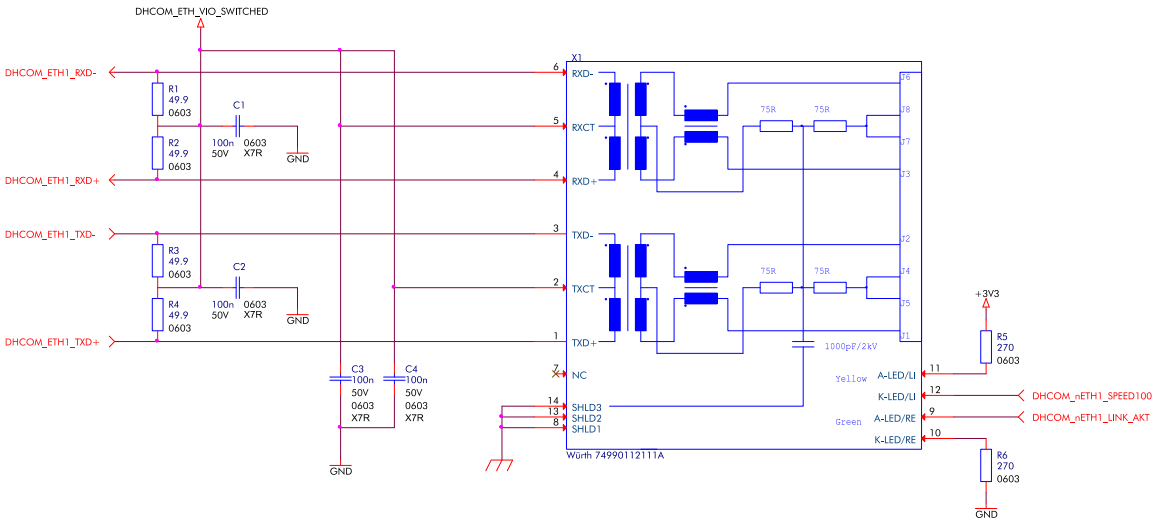


Figure 28: Ethernet connection

Note: The connection of the Ethernet LED outputs nETH1_LINK_LED and nETH1_SPEED_LED deserves special attention:

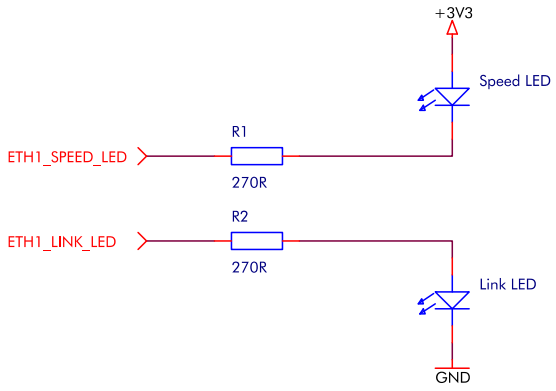


Figure 29: Ethernet LED connection

If the Ethernet LED pins are not used, they must nevertheless, as shown in Figure 29, have 10k pull-up and pull-down resistors.

Background: In addition to their LED function, the Ethernet PHY LEDs are used as reset configuration lines.

Layout routing guidelines:

The Ethernet data lines are to be routed as differential pairs with lengths equalised to within 0.25 mm. Furthermore, no stub lines may be connected to the data lines.

- Differential impedance: 100Ω ±15%
- Pair-to-pair pitch: min. 0,8mm
- Spacing to CLK signals: min. 1,5mm
- Maximum trace length between SODIMM-200 and magnetics: 100mm (keep it as short as possible)
- Maximum via count: 2
- The 49.9 ohm pull-up resistors on the differential lines, DHCOM_ETH*_RXD± and DHCOM_ETH*_TXD±, must be placed within 10mm of the SODIMM-200 connector. This ensures the transmit path is identical between TX and RX.
- Keep the RJ45 connector and the magnetics as close as possible.
- „Differential pairs" must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.
- A ground plane should be placed under the TX/RX pairs between the ethernet PHY and integrated RJ45 jack.
- A separate ethernet chassis ground should be placed under the RJ45 jack.
- The chassis ground should be connected to the rest of the PCB GND with capacitor stuffing options, which is useful for determining which values and location will provide the best EMI performance.

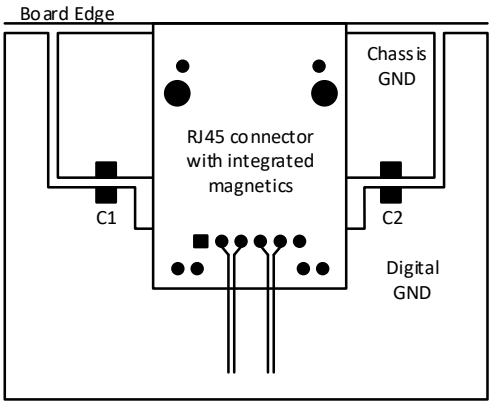


Figure 30: Ethernet Layout GND planes

3.14 Gbit Ethernet interface

Gbit Ethernet is available via RGMII interface on the high speed connector (DHCOM-X interface). The following figure shows an example of a Gbit ethernet connection:

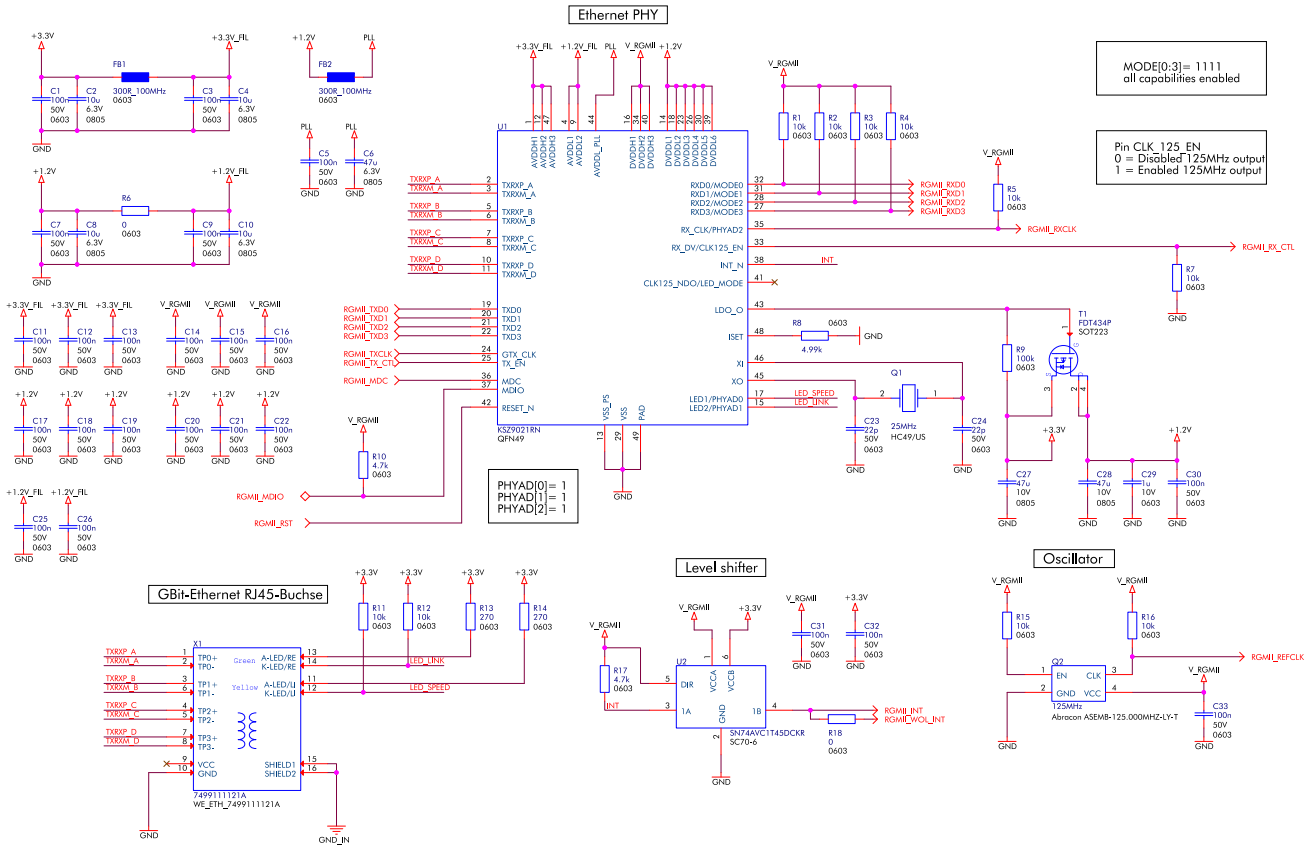


Figure 31: Gbit ethernet connection

High speed connector (DHCOM-X) pin name	Description	Pin number	IO Type	Voltage level
RGMII_TXCLK	RGMII transmit clock, 125 MHz digital	2	O	Vrgmii

RGMII_TXD0	RGMII transmit data 0	4	O	Vrgmii
RGMII_TXD1	RGMII transmit data 1	6	O	Vrgmii
RGMII_TXD2	RGMII transmit data 2	8	O	Vrgmii
RGMII_TXD3	RGMII transmit data 3	10	O	Vrgmii
RGMII_TX_CTL	RGMII transmit enable	12	O	Vrgmii
RGMII_RXCLK	RGMII receive clock, 125 MHz digital	1	I	Vrgmii
RGMII_RXD0	RGMII received data 0	3	I	Vrgmii
RGMII_RXD1	RGMII received data 1	5	I	Vrgmii
RGMII_RXD2	RGMII received data 2	7	I	Vrgmii
RGMII_RXD3	RGMII received data 3	9	I	Vrgmii
RGMII_RX_CTL	RGMII receive data valid	11	I	Vrgmii
RGMII_MDC	Management data clock	14	O	Vrgmii
RGMII_MDIO	Management data	13	IO	Vrgmii
RGMII_REFCLK	MAC reference clock input (125MHz)	16	I	Vrgmii
RGMII_RST	PHY reset	15	O	Vrgmii
RGMII_INT	PHY interrupt (active low)	18	I	**3V3**
RGMII_WOL_INT	PHY Wake-on-LAN interrupt (active low)	17	I	**3V3**
V_RGMII	Supply voltage output for external PHY IO voltage (max. 100mA)	20	PWR_O	Vrgmii

Table 7: RGMII interface

Note: The RGMII_INT and RGMII_WOL_INT nets are using 3V3 voltage level.

RGMII Layout routing guidelines:

- RGMII single ended impedance: 50Ω ±15%
- RGMII trace lengths equalised: within 0.25mm
- no stub lines
- Maximum trace length from DHCOM connector to ethernet PHY (RGMII interface): 60mm
- Spacing to CLK signals: min. 1.5mm
- Maximum via count: 2

PHY to magnetics Layout routing guidelines:

- PHY to magnetics differential impedance: 100Ω ±15%
- Differential pair lengths equalised: within 0.25mm
- Maximum via count: 2
- Pair-to-pair pitch: min. 0,8mm
- Max trace length between PHY and magnetics: 100mm (keep it as short as possible)
- Keep the RJ45 connector and the magnetics as close as possible
- „Differential pairs“ must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.
- A ground plane should be placed under the TX/RX pairs between the ethernet PHY and

integrated RJ45 jack.

- A separate ethernet chassis ground should be placed under the RJ45 jack.
- The chassis ground should be connected to the rest of the PCB GND with capacitor placement options, which is useful for determining which values and location will provide the best EMI performance.

3.15 PCIe

The PCIe Interface is available on the high speed connector (DHCOM-X interface). The DHCOM Standard features only one PCIe lane. The following figure shows an example connection to a mini PCIe connector:

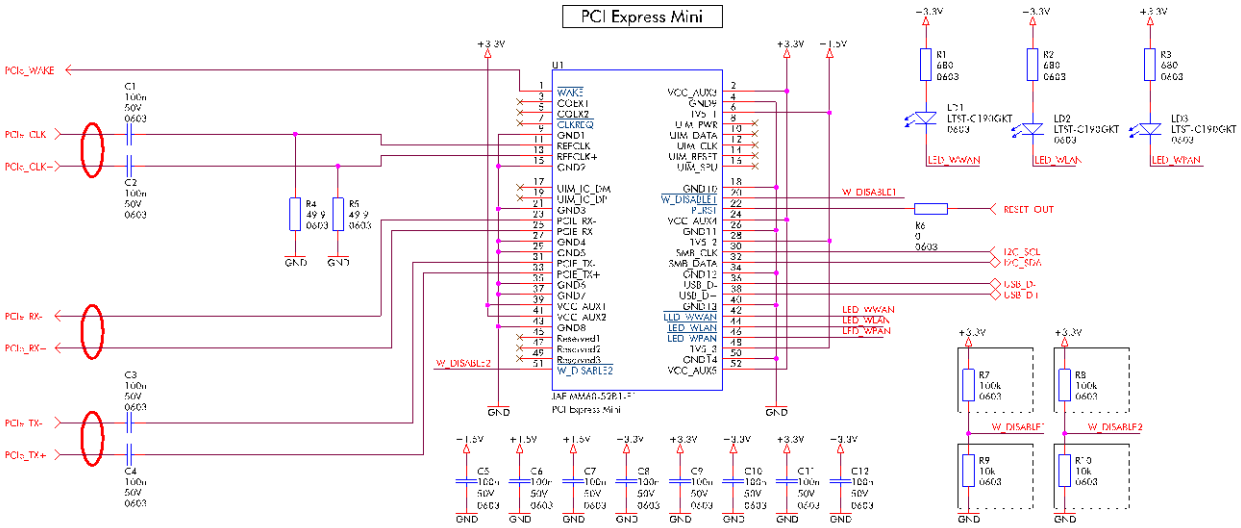


Figure 32: mini PCIe connection

PCIe Layout routing guidelines:

- Max. frequency:
  - Gen1: 1.25GHz
  - Gen2: 2.5GHz
- Differential Impedance: 100Ω ±15%
- Single ended impedance: 50Ω ±15%
- Trace lengths equalised within the diff. pairs: 1mm
- Trace length difference within a pair: 0.125mm
- no stub lines
- Maximum trace length from SODIMM-200 connector to PCIe slot connector: 100mm (keep it as short as possible)
- Spacing to other signals (especially clock signals): min. 1.5mm

- Pair-to-pair pitch: min. 0,5mm
- Maximum via count: 2
- Place the AC coupling capacitors as close as possible to the transmitter side.
- „Differential pairs“ must be routed over a solid ground or VCC plane to maintain a controlled impedance over the entire trace route.

Notes:

- **DHCM-iMX6-01D2:**
  The PCIe reference clock PCIE_REFCLK+/- can’t pass PCIe Gen2 compliance test. Therefore we recommend using external PCIe 2.0/3.0 clock generator, like Silicon Labs SI52144-A01AGM.

4 Cooling Solution

4.1 Description

This chapter relates to the DHCOM core modules, that need to be cooled during operation.

DHCOM CPU Module	Cooling necessary?
i.MX25x	No
AM35x	No
i.MX6UL(L)	No
AM335x	**Depends on application**
i.MX6 Solo	**Depends on application**
i.MX6 DualLite	**Depends on application**
i.MX6 Dual	**Yes**
i.MX6 Quad	**Yes**
SD600E	**Yes**

Table 8: Cooling necessary?

Modern multi-core CPUs such as the i.MX6 from NXP must have passive cooling. This results in the following problems:

- Heat sink is required
- Heat sink must be assembled on the hardware
- Additional material and manufacturing costs

For this reason, DH electronics GmbH uses an innovative cooling solution that is intended to avoid the above-mentioned disadvantages.

The solution is dependent on the specific DHCOM core module and the SODIMM-200 connector used. These two dependencies define the distance between CPU and Mainboard PCB. This distance is necessary, because the heat of the CPU is transferred with a gap or copper pad to the Mainboard PCB.

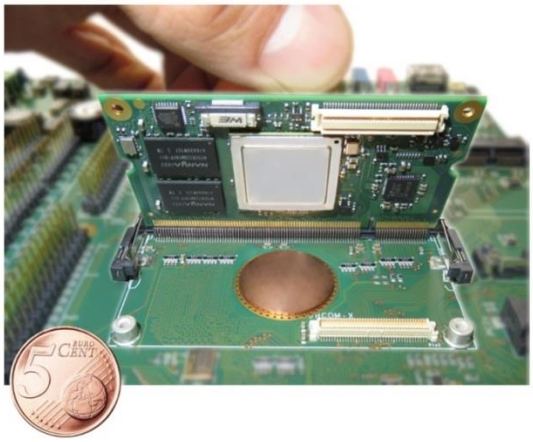


Figure 33: 5 Cent cooling solution

On the mainboard there are now two ways of distributing the heat with thermal vias:

1. **Dissipation into the inner layers (GND)**

   The heat is led into the inner layers of a PCB (min. 4 layer PCB) via thermal vias. These inner layers are flooded with copper. Typically, a connection is made to the GND or VCC supply. The entire PCB heats up via these copper planes and therefore gives off the CPU heat into the surrounding area.

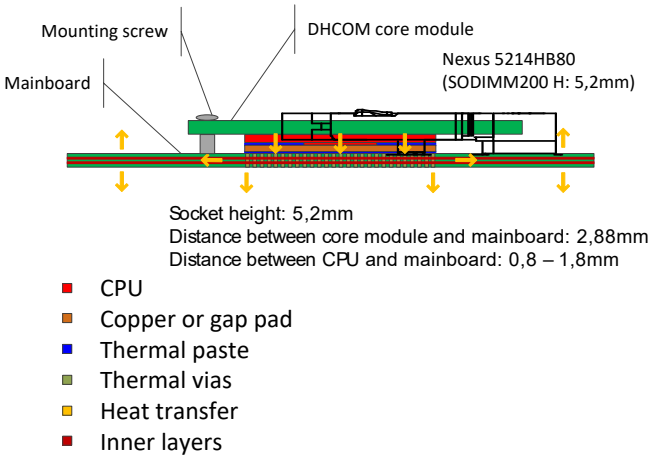


Figure 34: Dissipation into the inner layers

Attention: Components on the mainboard PCB will be heated up with this solution.

2. **Dissipation on the rear of the mainboard**

   If housing is available in the final application to which the heat can be dissipated, it would be possible to lead the heat to the bottom of the mainboard PCB (thermal vias) and dissipate it with an aluminum or copper block to the housing.

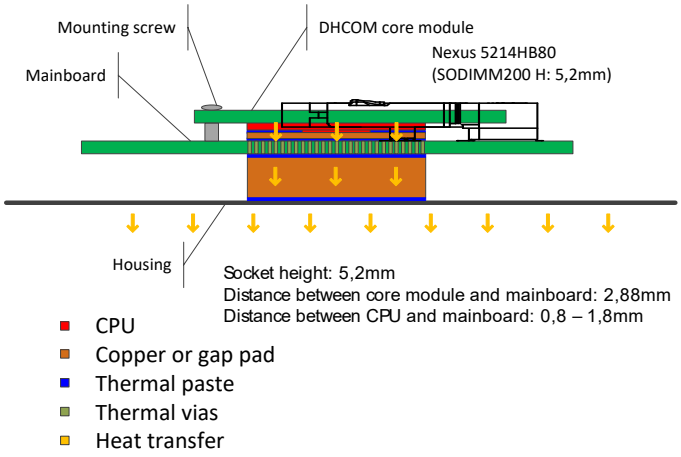
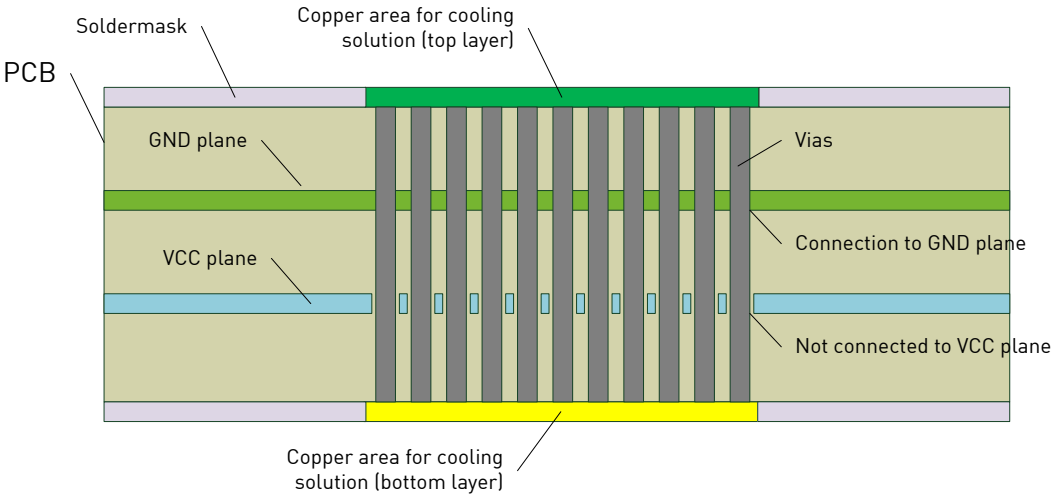


Figure 35: Dissipation on the rear of the mainboard

4.2 Implementation

For the cooling solution it is necessary to provide a thermal copper area on the mainboard PCB which is connected to the internal ground planes (dissipation into the inner layers) or to a second thermal copper area on the bottom side of the PCB (dissipation on the rear of the mainboard). It is also necessary to provide steel spacers on the mainboard for the final fixation of the core module.



Note: Area for heatsink or graphite foil connection.

Figure 36: Cooling solution - PCB layer stack

The position of the thermal copper area and steel spacers is shown in Figure 50: Mainboard Placement on page 47.

The following table shows the different distances between CPU and mainboard PCB.

CPU Type	SODIMM-200 connector height	Distance between CPU and Mainboard

CPU Type	SODIMM-200 connector height	Distance between CPU and Mainboard
AM335x	5,2mm	1,58mm
AM335x	9,2mm	5,58mm
i.MX6 Solo	5,2mm	1,43mm
i.MX6 Solo	9,2mm	5,43mm
i.MX6 DualLite	5,2mm	1,43mm
i.MX6 DualLite	9,2mm	5,43mm
i.MX6 Dual (metal housing)	5,2mm	1,03mm
i.MX6 Dual (metal housing)	9,2mm	5,03mm
i.MX6 Quad (metal housing)	5,2mm	1,03mm
i.MX6 Quad (metal housing)	9,2mm	5,03mm

Table 9: CPU to mainboard distance

For the next step it is necessary to select a suitable TIM (thermal interface material) for the CPU used and SODIMM-200 connecter.

CPU Type	SODIMM-200 connector height	Copper pad height	Gap-Pad
i.MX6 Solo	5,2mm	1,25mm	19x19mm Bergquist GP3500ULM-G-0.080-12
i.MX6 DualLite	5,2mm	1,25mm	19x19mm Bergquist GP3500ULM-G-0.080-12
i.MX6 Dual (metal housing)	5,2mm	0,85mm	19x19mm Bergquist GP3500ULM-G-0.060-12
i.MX6 Quad (metal housing)	5,2mm	0,85mm	19x19mm Bergquist GP3500ULM-G-0.060-12

Table 10: TIM material

4.2.1 Copper Pad

When using a copper pad as thermal interface material (TIM), a thermally conductive paste is necessary to minimize the thermal resistance between CPU and mainboard PCB. Therefore DH electronics recommends **heat transfer compound** from **RS components (Item number: 554-311)**. The proper implementation of the heat transfer compound is shown in the following images (Figure 37 and Figure 38). After the application of the heat transfer compound the CPU-carrier board **must be pushed down in the centre** (illustrated in Figure 39) into the SODIMM-200 connector.

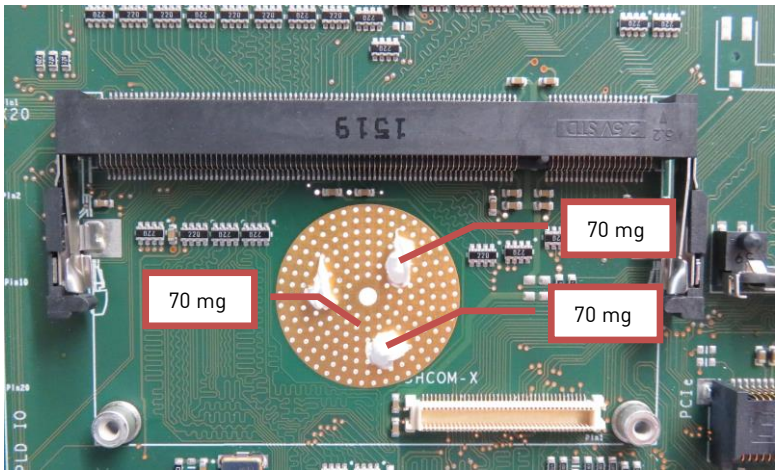


Figure 37: Apply heat transfer compound to Mainboard PCB

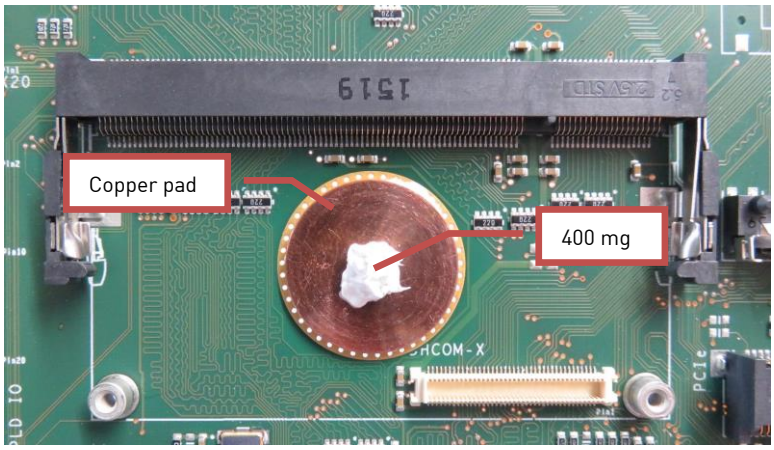


Figure 38: Apply heat transfer compound to copper pad

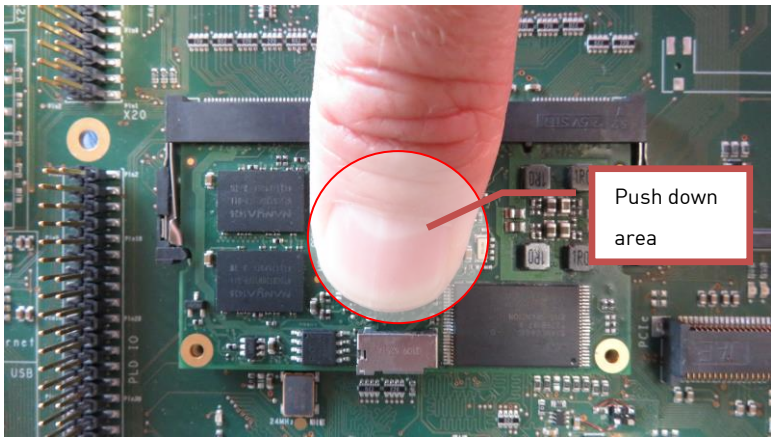


Figure 39: Core module push down area

4.2.2 Gap-Pad

Instead of a copper pad DH electronics also recommend the usage of Bergquist GP3500 ULM. Notice that the Young's modulus of the GP3500 ULM is very low in comparison with other suitable gap-pads for this purpose.

This calls for low mechanical tension on the main PCB and CPU-carrier board. The proper implementation of the gap-pad is shown in Figure 40. After the application of the gap-pad the CPU-carrier board **must be pushed down in the centre** (illustrated in Figure 39) into the SODIMM-200 connector.

Important: Don't remove the core module after assembly process! In this case a new gap-pad must be used.

Figure 40: Apply Gap-Pad

4.3 Comparison gap-pad to copper pad

The impact of the different thermal interface implementations on the heat management of the CPU is shown in the bar charts (Figure 41, Figure 42) below.

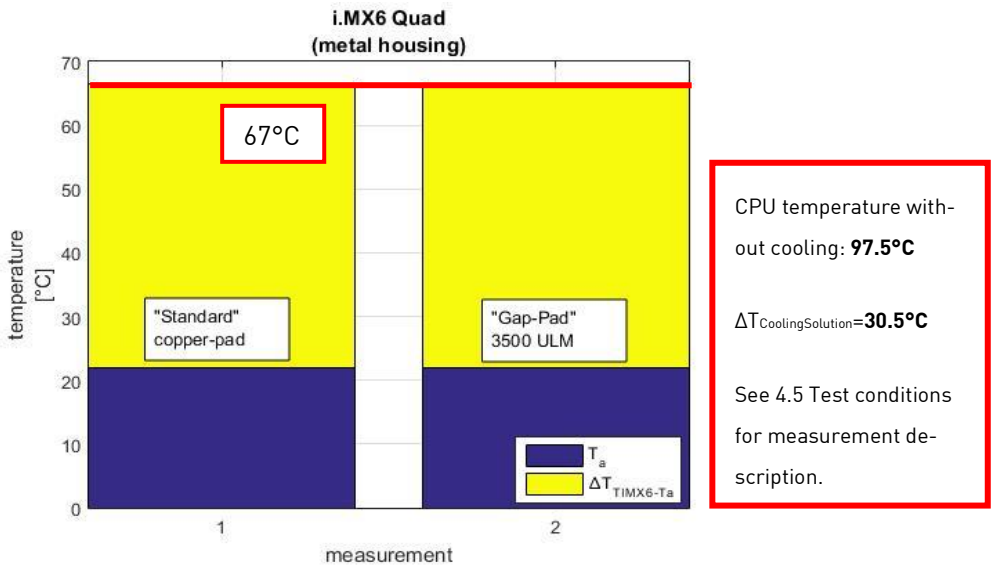


Figure 41: thermal management i.MX6 Quad

Because of the following advantages **DH electronics would recommend the usage of a gap-pad** instead of the copper pad:

- Easier to assemble
- No aging (instead of thermal paste)
- Compensates tolerances better than thermal past and copper pad
- Easy disassembling

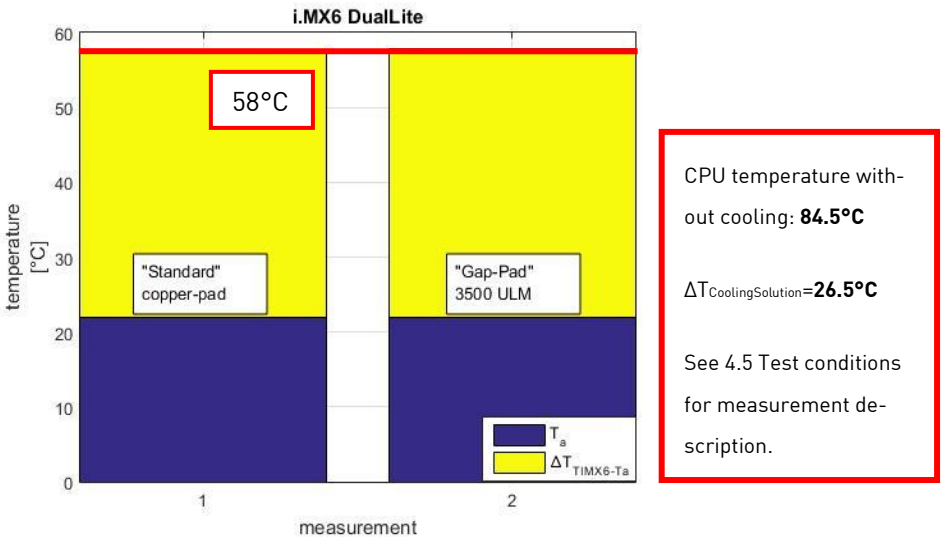


Figure 42: thermal management i.MX6 DualLite

4.4 Further cooling possibilities

If further cooling of the CPU is required:

➔ Highly thermal conductive graphite foil (PGS) offers an easy and effective method of improving the heat dissipation from the CPU.

The application of graphite foil to the bottom side of the mainboard PCB (improves the temperature spread) is illustrated in Figure 43. The experimental assembly on which the measurements are based is shown in (Figure 44).

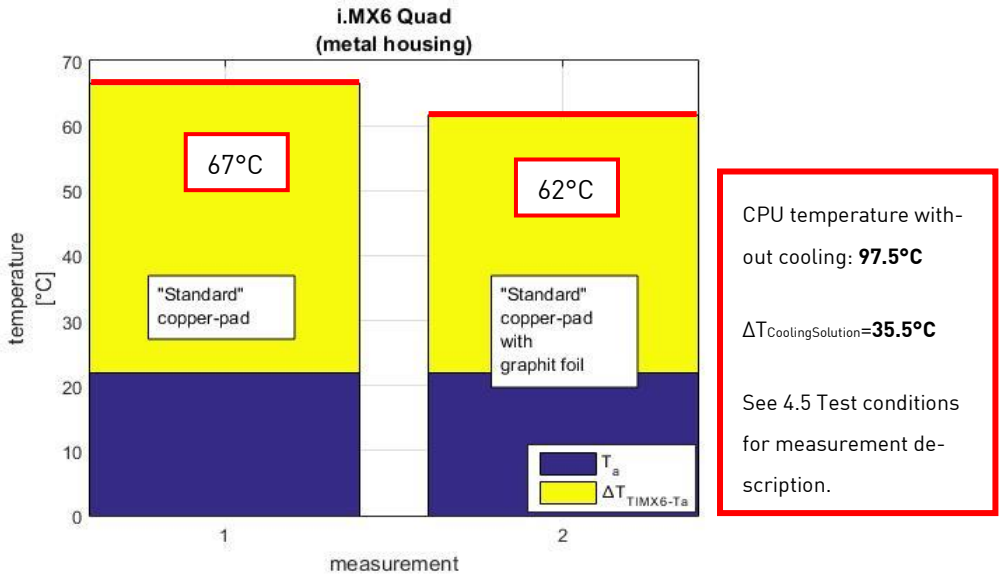


Figure 43: Thermal impact PGS foil (i.MX6 Quad)

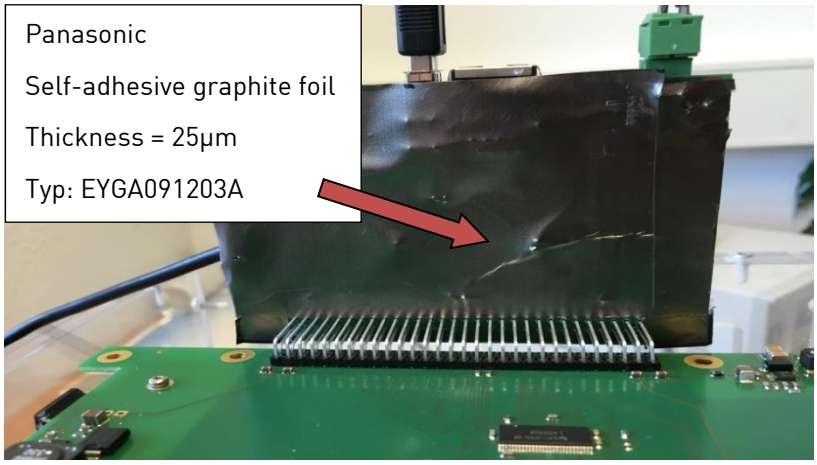


Figure 44: Experimental assembly

Another thermal improvement is possible by using the graphite foil as "thermal bridge" to an extern heat sink or housing. The results are shown in Figure 45. The measured assembly is shown in Figure 46.

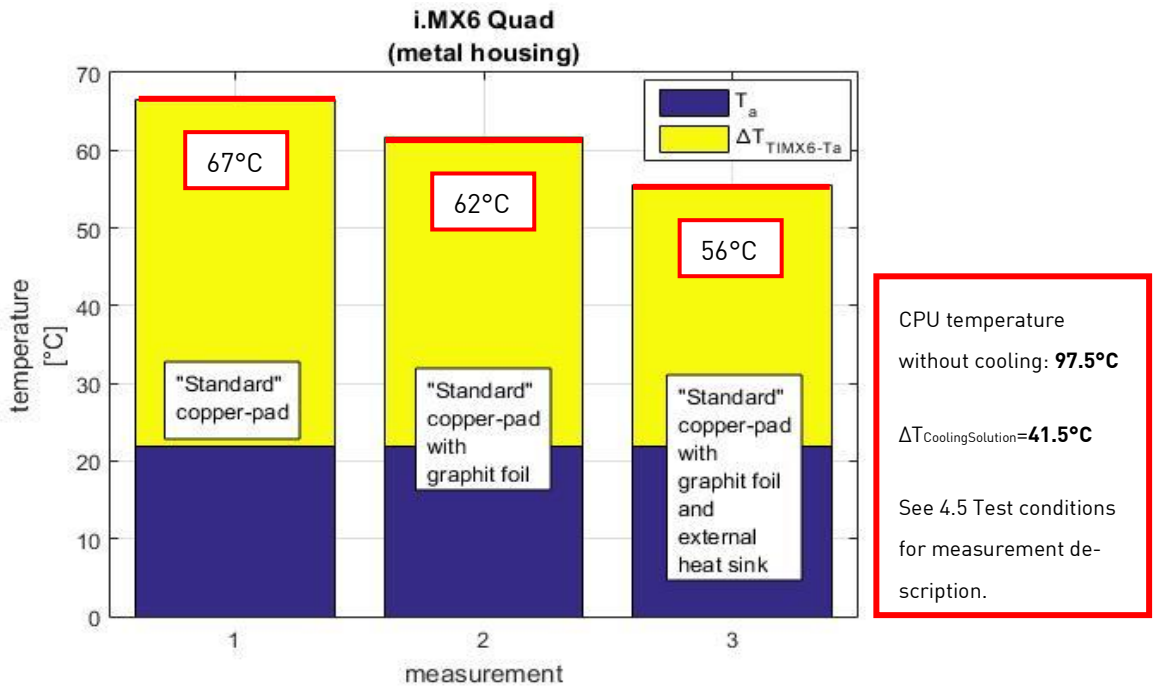


Figure 45: PGS foil as thermal bridge

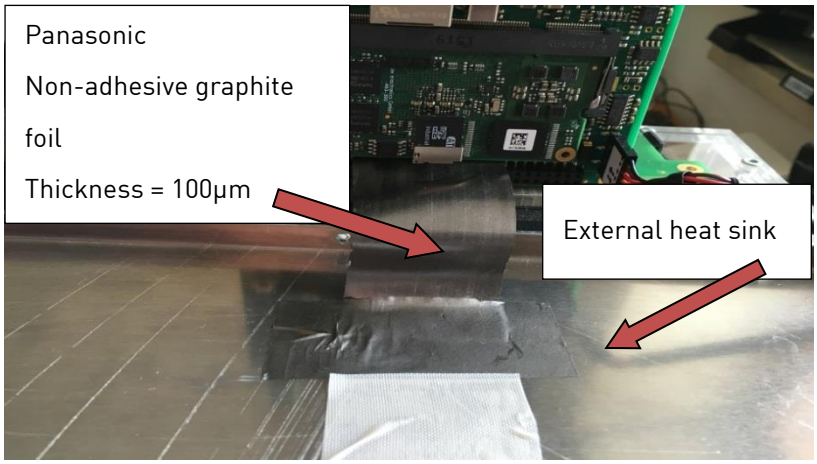


Figure 46: Carrying the heat

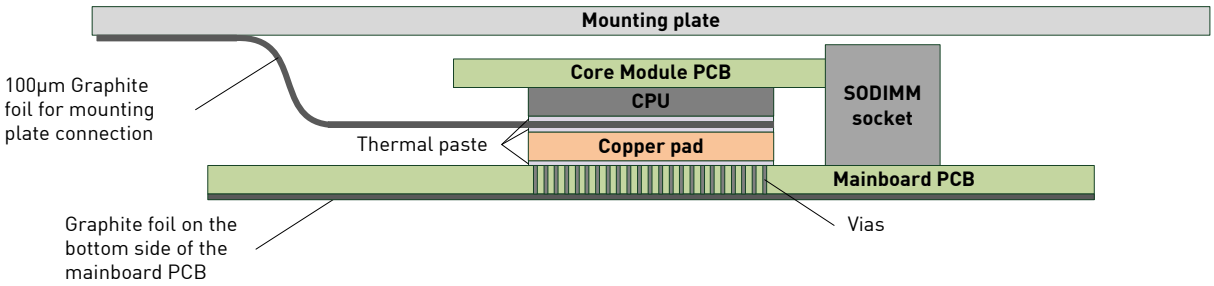


Figure 47: Graphite foil to mounting plate connection

In general graphite foil can be used in a variety of different implementations. For further information please read the Panasonic datasheets (Basic Properties and Application Examples of PGS Graphite Sheet).

4.5 Test conditions

All above described measurements are done with the same test conditions:

- Linux Vendor Kernel 3.10.17 for DHCOM i.MX6
- PMIC support and DVFS activated
- CPU clock frequency: 800MHz
    - `echo 800000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_max_freq`
    - `echo 800000 > /sys/devices/system/cpu/cpu1/cpufreq/scaling_max_freq`
    - …
- Running stress-ng test to produce CPU load
    - Quad Core: `stress-ng --cpu 4 --vm 1 --vm-bytes 128M -v`
    - DualLite: `stress-ng --cpu 2 --vm 1 --vm-bytes 128M -v`
- Running direct GLX demo (glxheads) from Xfce desktop to generate GPU load
- CPU temperature measurement is done with the i.MX6 internal temperature sensor
    - `cat /sys/class/thermal/thermal_zone0/temp`

5 Mechanical

5.1 Fixation

1. Without cooling connection and high-speed connector (DHCOM-X)

With a DHCOM standard module, attachment with screws is not necessary, but can take place using the following holes for special usage cases:

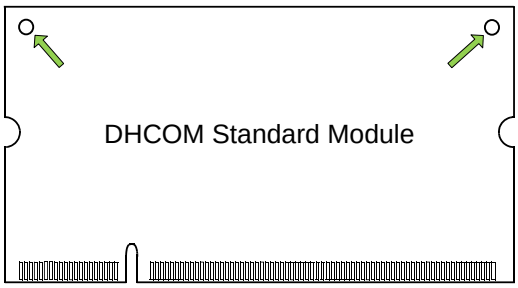


Figure 48: DHCOM attachment

2. With cooling connection or high-speed connector (DHCOM-X)

With a DHCOM-X (with high-speed connector) core module or with DHCOM cooling solution, attachment is needed in order to ensure that the contacting of the Molex connector or/and the thermal connection to mainboard is provided, i.e. it must be screwed on at the attachment points (see locations marked in red in the following drawing).

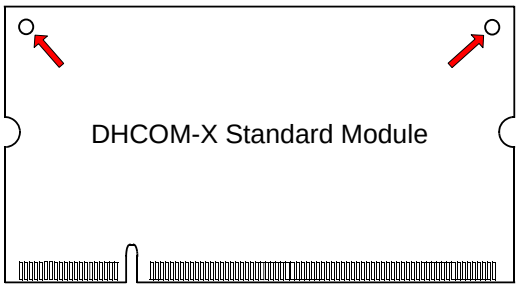


Figure 49: DHCOM-X attachment

The position of the steel spacers is shown in Figure 50: Mainboard Placement on page 47.

5.2 Mainboard Placement

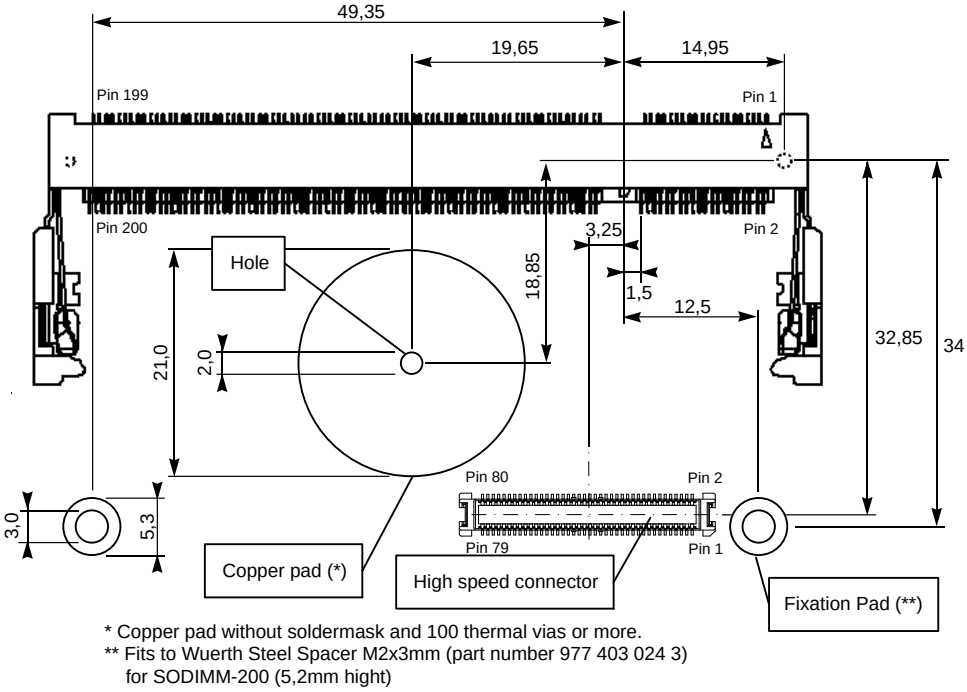


Figure 50: Mainboard Placement

5.3 Carrier Board Space Requirements

The required PCB area for the module is depended to the DHCOM module. Two different sizes are available:

- DHCOM standard size: 67,6mm x 36.7 mm (length x width)
- DHCOM **extended** size: 67,6mm x 45.7 mm (length x width)

DHCOM CPU Module	Size
i.MX25x	DHCOM standard size
AM35x	DHCOM standard size
i.MX6UL(L)	DHCOM standard size
AM335x	DHCOM standard size
i.MX6 Solo	DHCOM standard size
i.MX6 DualLite	DHCOM standard size
i.MX6 Dual	DHCOM standard size
i.MX6 Quad	DHCOM standard size
SD600E	**DHCOM extended size**

Table 11: DHCOM module size overview

Notes:

- The placement for high speed connector, cooling pad and fixation points is for both sizes the same.

- DHCOM extended size module can be used in PDK2 evaluation board.
- DHCOM extended size module can NOT be used in combination with picoITX2 board.

The following figure shows the DHCOM dimensions of both available sizes:

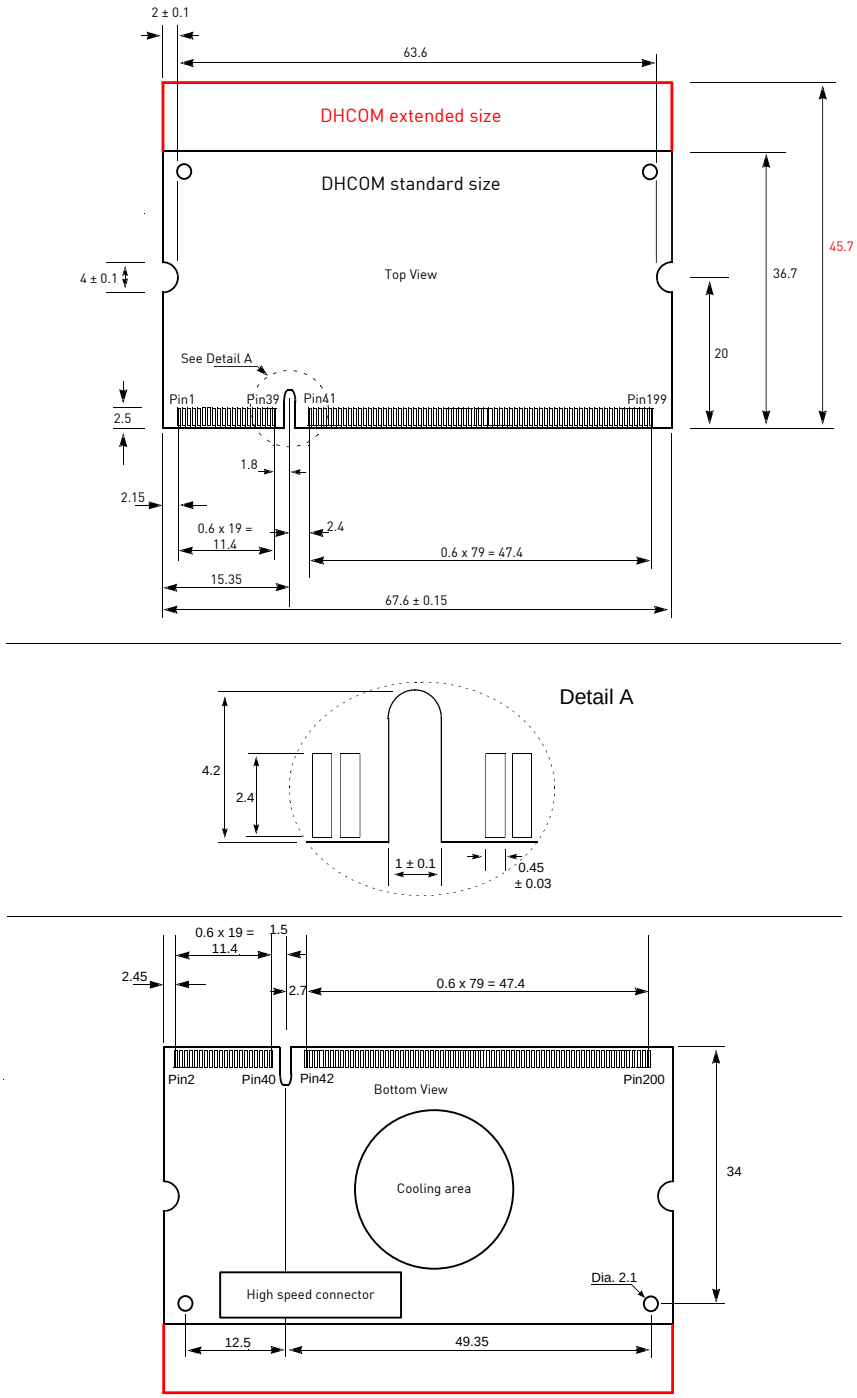


Figure 51: DHCOM dimensions

6 System voltages

Voltage	i.MX25	i.MX6UL(L)	AM35x	AM335x	i.MX6	SD600E
VCC (Vin)	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V	3.3V – 5.5V
V_{bat}	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V	1.3V – 4.0V
V_{sysbus}	1.8V	- (3.3V)	3.3V	- (3.3V)	3.3V	- (1.8V)
V_{disp}	3.3V	3.3V	3.3V	3.3V	3.3V	1.8V
V_{cam}	3.3V	3.3V	3.3V	3.3V	3.3V	1.8V
V_{IO}	3.3V	3.3V	3.3V	3.3V	3.3V	1.8V
$V_{ETH_VIO_SWITCHED}$	3.3V	3.3V	3.3V	3.3V	3.3V	1.8V
USB_OTG_VBUS	5.0V	5.0V	5.0V	5.0V	5.0V	5.0V

Table 12: Voltage groups

For power supply limitations, please see the DHCOM module user manual.

7 PDK Display adapter interface

The display adapter interface of the DHCOM Premium Developer Kit can be used to connect any display via a newly developed display adapter board. The circuit diagram symbol of the display adapter connector for OrCAD capture can be downloaded from the following link:

http://xlon.de/wiki/images/4/4a/DHCOM_schematic_symbol_R02.zip

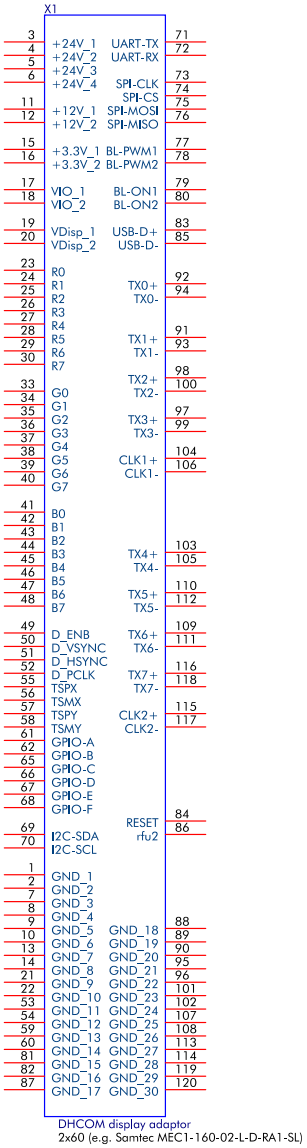


Figure 52: Display adapter circuit diagram symbol

8 Schematic

8.1 SODIMM-200

The circuit diagram symbol of the SODIMM-200 connector for OrCAD capture can be downloaded from the following link:

http://xlon.de/wiki/images/4/4a/DHCOM_schematic_symbol_R02.zip

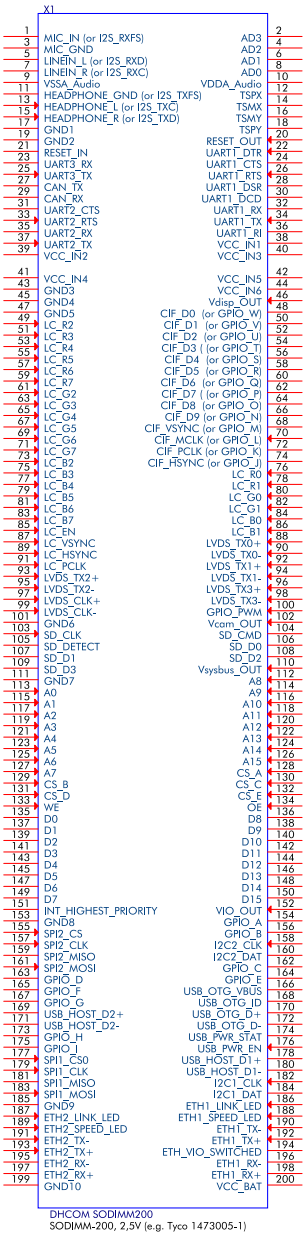


Figure 53: SODIMM-200 circuit diagram symbol

8.2 High speed connector (DHCOM-X)

The circuit diagram symbol of the Molex high speed connector (DHCOM-X) for OrCAD capture can be downloaded from the following link:

http://xlon.de/wiki/images/4/4a/DHCOM_schematic_symbol_R02.zip

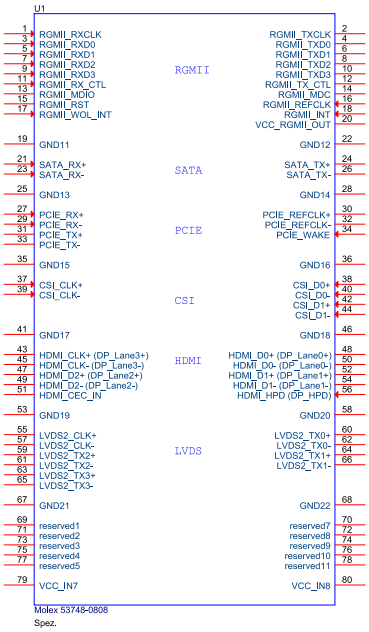


Figure 54: High speed connector circuit diagram symbol

9 Connectors

9.1.1 SODIMM-200 (DHCOM)

A DHCOM standard module is designed for use in a 2.5V DDR2 SODIMM-200 memory socket.

DHCOM-X note: DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector.

The following SODIMM-200 sockets have been tested and approved:

Manufacturer	Description	Article number
Nexus Components http://www.nexus-de.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	DMD-200-RSE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	1473005-1
FCI http://www.fci.com/	▪ Plug height: 5.2 mm ▪ Max. main board component height below the module: 1.0 mm	59354-052FSLF
Nexus Components http://www.nexus-de.com/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	5214HB52
E-tec Interconnect http://www.e-tec.ch/v3/	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	DMD-200-RPE9-55
Tyco Electronics http://www.tycoelectronics.com	▪ Plug height: 9.2 mm ▪ Max. main board component height below the module: 5.0 mm	1612618-1

Table 13: SODIMM-200 sockets

9.1.2 Molex (DHCOM-X)

A Molex (http://www.molex.com/) SlimStack connector is provided for contacting the DHCOM-X connector. DHCOM-X contacting is only possible in combination with a 5.2 mm SODIMM-200 connector. A 9.2 mm high SODIMM-200 socket cannot be used for DHCOM-X.

SODIMM-200 socket height	Description	Article number
5.2mm	0.50mm Pitch SlimStack™ Plug, Surface Mount, Dual Row, Vertical, 3.00mm Stack Height, 80 Circuits	Molex 53748-0808
9.2mm	Not available	Not available

Table 14: DHCOM-X sockets

9.1.3 JTAG

The JTAG connector is placed on the DHCOM core module and can be contacted with a 10-pin FFC cable.

Manufacturer	Description	Article number
Wuerth Elektronik http://www.we-online.com	0.50 mm flat flexible cable Type 1 WR-FPC	687 610 050 002
Molex http://www.molex.com/	0.50mm flat flexible cable Type A	982660097

Table 15: FFC Cable