Schematics

Company: DH electronics GmbH

Project: DHeva01

SRAM Testplatine

Version: 460-200 (Rev. 1.0)

12.11.2012

Variants: Standard

Core

Temperatur range:

0 .. +50 °C

Changelog:

[SG][Page1]: Added front page
[SG][Page2]: Added GND and VCC connection
[SG][Page2]: Removed TA3, TA4 and TA5

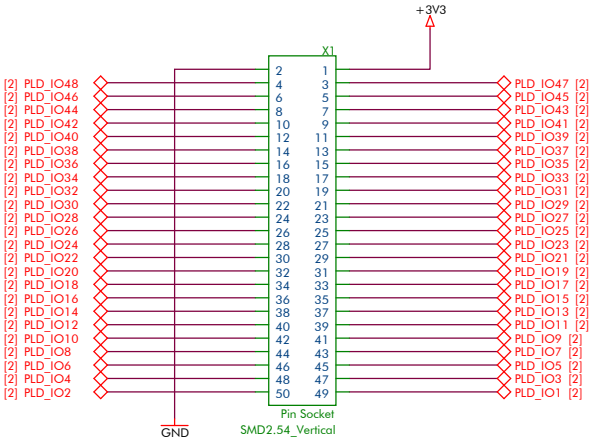
Notes:

Created: SG

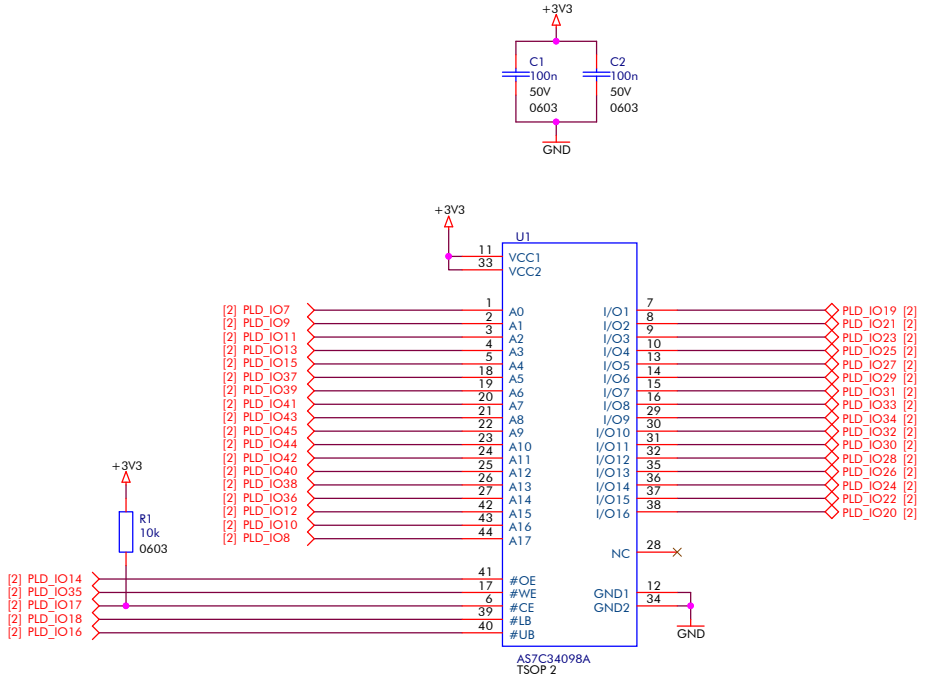
Content:

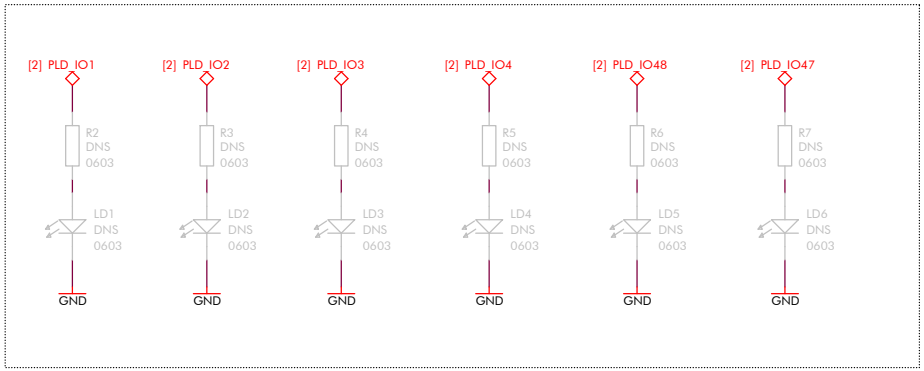
ELECTRONICS
Am Anger 8
D-83346 Bergen

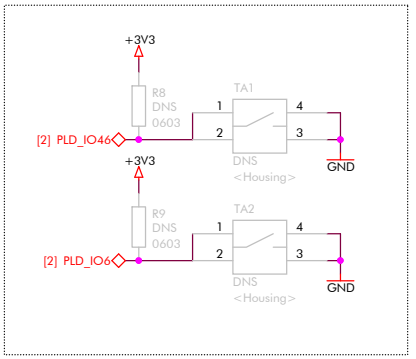
Projekt: SRAM Testplatine
Beschreibung: Frontpage
Variante: Standard
Zeichnungsnummer: 460-200 | Freigabe: <Date> | Version: 1V0
Zuletzt geändert: Friday, November 16, 2012 | Seite: 1 / 2



PLD_IO5 not used in this application







ELECTRONICS

Am Anger 8
D-83346 Bergen

Projekt
SRAM Testplatine

Beschreibung
Memory

Variante	Standard		
Zeichnungsnummer	460-200	Freigabe: <Date>	Version 1V0
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