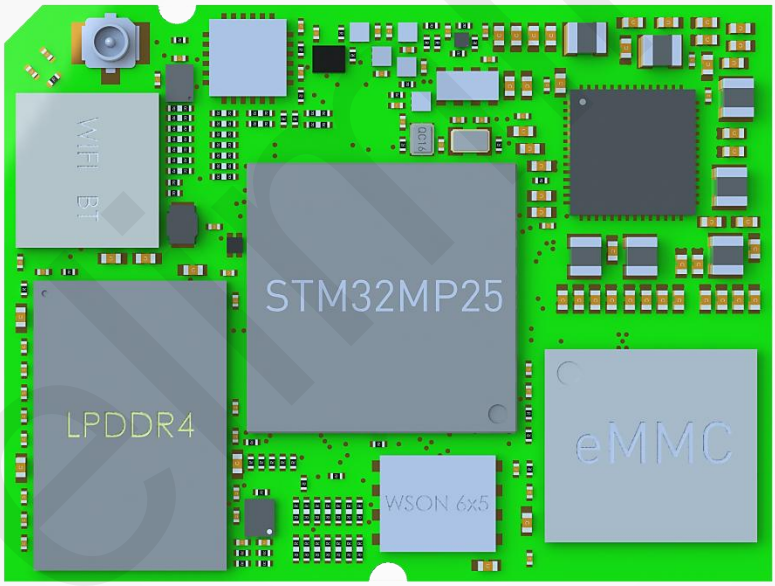
DHCOS STM32MP2x

User manual



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History

Version	Data	Description of changes	Name
Rxx	27.05.2025	First draft	AG

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2 Abbreviations

- BGA = Ball grid array
- BSP = Board Support Package
- CLK = Clock
- DHCOS = DH compatible on solder
- DHSBC = DH single board computer
- EMC = Electro magnetic compatibility
- ESD = electrostatic discharge
- fps = Frames per second
- GPU = Graphics Processing Unit
- HW = Hardware
- I/O = Input/output
- LCD = Liquid Crystal Display
- LGA = Land grid array
- MBC = Must be connected
- MSL = Moisture sensitivity level
- Msps = Mega samples per second
- NC = No connect
- OE = Open Embedded
- PCB = Printed Circuit Board
- PD = Pull-down
- PnP = Pick and place
- PU = Pull-up
- RFU = Reserve for Future Use
- RGB = Red Green Blue parallel display
- RH = Relative humidity
- RST = Reset
- RTC = Real-Time Clock
- SAC = SnAgCu (Tin-silver-copper)
- SMT = Surface mounted technology
- SWD = Serial wire debug
- TBD = To be defined
- TPM = Trusted Platform Module

3 Introduction

3.1 Hardware

The solderable DHCOS-STM32MP2-01LG System on Module based on the powerful STM32MP25x processor from STMicroelectronics combines flexibility and pin-compatibility. Equipped with dual Cortex-A35 cores with a clock frequency of 1.2 GHz and an additional Cortex-M33 co-processor with 400 MHz, the DHCOS STM32MP2 offers powerful computing performance with optimized energy efficiency. Thanks to LPDDR4 RAM, SPI boot flash, eMMC flash, GBit Ethernet and integrated WiFi and Bluetooth, comprehensive connectivity is guaranteed. Support for a 3D GPU with extended graphics functions for displays, videos and cameras ensures demanding multimedia applications. The use of the STPMIC1 power management IC enables versatile low-power modes, ideal for energy-efficient applications. Another highlight is the mainline Linux support, which enables easy integration and software updates. With a compact size of just 30 x 40 mm, the SOM is perfect for space-saving designs without compromising on performance. Thanks to the guaranteed long-term availability of 10+ years, the DHCOS STM32MP2 offers maximum investment security - an ideal choice for industrial and demanding IoT applications.

3.2 Software

Currently, the DHCOS-STM32MP2-01LG module is available with the Embedded Linux operating system based on OE/Yocto based. In addition, the DHSBC STM32MP25 reference design is also up streamed to mainline Linux and U-Boot. And the SOM is also maintained over the years based on this board.

3.3 Main characteristics

Note: The following list describes the features of the DHCOS STM32MP2x System on Module in relation to the DHCOS standard. If you break from the DHCOS standard, other functions can be realized, but you will lose compatibility with the DHCOS standard. Please contact DH if you have any questions.

- Dual Cortex®-A35 up to 1.5 GHz
- Single Cortex®-M33 up to 400 MHz
- Power efficient and cost optimized application processor
- Power management: STPMIC25D
- Crypto Engine, Secure Boot, "On-the-fly" DDR encryption/decryption (AES-128)
- 3D GPU: VeriSilicon® - Up to 150 Mtriangle/s, 900 Mpixel/s with OpenGL® ES 3.1 - Vulkan 1.3 and OpenCL™ 3.0, OpenVX™ 1.3 support
- Neuronal Processing Unit (NPU) VeriSilicon® with up to 900 MHz and 1.35 TOPS

- Video decode / encode Unit H264 up to 1080p60
- Quad SPI boot flash: 4 MByte
- LPDDR4 memory (32 bit with LPDDR4-2400): 1 / 2 / 4 GByte
- eMMC memory (8 bit with HS200 support): 4 / 8 / 16 / 32 GByte
- EEPROM 32 kByte
- Ethernet: 2x Gbit via RGMII, IEEE 1588v2, TSN, 2x MDIO (3rd Gbit interface on request)
- I2S / SAI: 1x
- CAN: 2x FDCAN, 1x TTCAN
- UART: 4x UART up to 12.5 MBit/s (1x serial console and 3x UART with CTS/RTS)
- SPI: 1x up to 50 MBit/s
- QuadSPI: 1x up to 120 MHz (single, dual and quad communication)
- I2C™: 2x
- MMC/SD: 2x SDIO 4.0 / SD 3.01 / eMMC 5.1
- USB Host: 1x USB 2.0 HS
- USB Type-C: 1x USB 3.0 with 5Gbps, Operation mode USB 3.2 Gen 1x1 (Supported Interfaces: USB-A, USB-C and microUSB)
- Display RGB: 18-bit RGB666 up to FHD (1920 × 1080) @60 fps
- MIPI-DSI: 4-lanes up to 2.5 Gbit/s, up to QXGA (2048 × 1536) @60 fps
- LVDS: Dual Link, 2x 4-lane LVDS, up to 1.1 Gbit/s per lane, up to QXGA (2048 × 1536) @60 fps
- MIPI-CSI2: 1x 2-lanes up to 2.5 Gbit/s, 5 Mpixels @30 fps
- PCIe: 1x 1-lane PCI Express Gen2 up to 5 Gbit/s
- PWM: 2x PWM out, 16 Bit
- ADC: 2x 12 Bit ADC with internal or external voltage reference
- WiFi and Bluetooth® via Murata 2FY module with U.FL connector
    - Infineon CYW55513 Chipset for IEEE802.11a/b/g/n/ac/ax with Tri band 2.4 GHz, 5 GHz and 6 GHz
    - Compliant with Bluetooth specification v5.4 BR/EDR/LE
- Temp. compensated RTC RV-3032-C7
- GPIOs: 15x
- Boot mode: 4x, UART/USB, Serial NOR, eMMC, SD-Card, Development boot
- Debug interface: JTAG interface
- Power Control signals: Reset_In, Reset_Out Power-Good and Power-Button
- Integrated USB Type-C Power Delivery controller
- Industrial temperature range (-40°C to +85°C)

3.4 Further technical information

Beside this manual, please also have a look at the ST application note **AN5489** "**Getting started with STM32MP23/25xx MPUs hardware development**". This document shows how to use the STM32MP25 series and describes the minimum hardware resources required to develop a carrier board based on those MPU products.

3.4.1 STM32MP25 processor

Data sheets and technical documents can be found at
https://wiki.st.com/stm32mpu/wiki/STM32MP25_resources

3.4.2 STPMIC25D power manager

Data sheets and technical documents can be found at
https://wiki.st.com/stm32mpu/wiki/STM32MP25_resources

3.4.3 RV-3032-C7 real time clock

Data sheets and technical documents can be found at https://www.microcrystal.com/en/products/real-time-clock-rtc-modules/rv-3032-c7/

3.4.4 2FY Wi-Fi®/Bluetooth module

Data sheets and technical documents can be found at https://www.murata.com/en-eu/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type2fy

3.4.5 M24256E EEPROM

Data sheets and technical documents can be found at https://www.st.com/en/memories/m24256e-f.html

4 Hardware overview

4.1 Block diagram

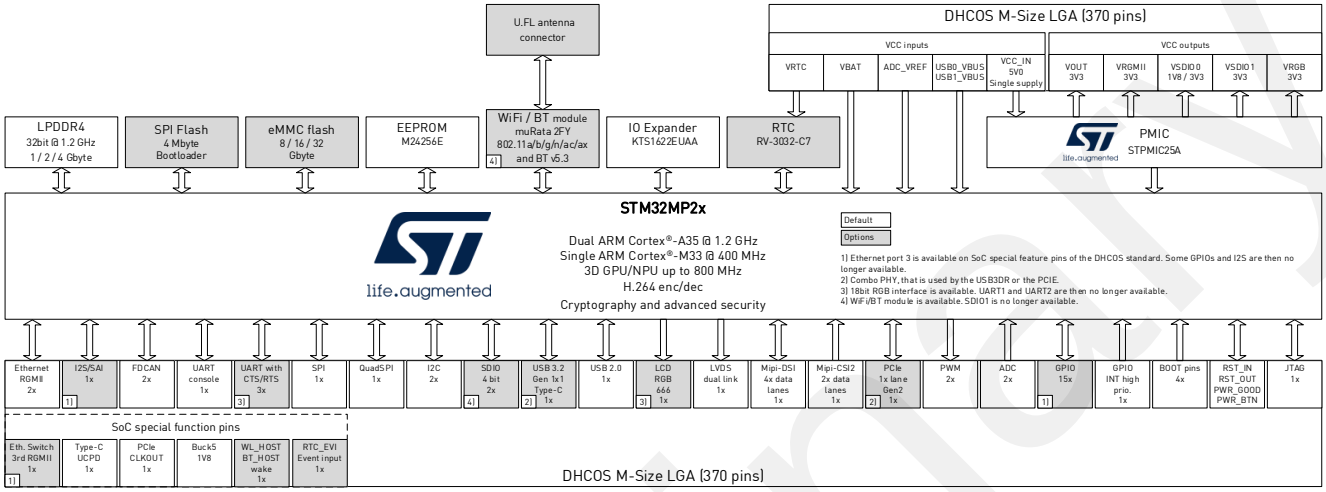


Figure 1: DHCOS-STM32MP2-01LG block diagram

4.2 Configuration overview

DHCS-CPU-Cxxx-Rxxx-EE[-F[P]xxxx][-SPIxx][-RTC][-WBT][-RGB][-PCIe/USB3][-ETH3]-X-01LG	
CPU	**STM32MP257C**: 2xCortex-A35 @ 1.2GHz, Cortex-M33 @ 400MHz, 3xEthernet (2+1 switch), 3xFD-CAN, LVDS/DSI, H.264, 3D GPU, AI / NN, Secure Boot, Cryptography, DRAM enc/dec, PKA **STM32MP255C**: 2xCortex-A35 @ 1.2GHz, Cortex-M33 @ 400MHz, 2xEthernet, 3xFD-CAN, LVDS/DSI, H.264, 3D GPU, AI / NN, Secure Boot, Cryptography, DRAM enc/dec, PKA **STM32MP253C**: 2xCortex-A35 @ 1.2GHz, Cortex-M33 @ 400MHz, 2xEthernet, 3xFD-CAN, Secure Boot, Cryptography, DRAM enc/dec, PKA Note: Please contact us for A-Type devices without Secure Boot and Cryptography support.
Cxxx	1.2 GHz: C120 Note: Please contact us for 1.5 GHz F-Type devices: C150
Rxxx	1024 Mbyte: R102, 2048 Mbyte: R204, 4096 Mbyte: R409
EE	256 kbit EEPROM
X	Industrial temperature range (-25 °C - 85 °C): I Notes: - Industrial temperature range for eMMC and LPDDR4 version is -25 °C - 85 °C. Please contact us for -40 °C - 85 °C. - Please contact us commercial temperature range (0 °C - 70 °C): C
01LG	DHCOS Revision, LGA connection
Options	
[-F[P]xxxx]	4096 Mbyte eMMC: F0409, 8192 Mbyte eMMC: F0819, 16384 Mbyte eMMC: F1638 Notes: - Please contact us for eMMC with pSLC support: FPxxxx - Other sizes on request
[-SPIxx]	4 Mbyte SPI boot flash: SPI04 Note: Other sizes on request.
[-RTC]	Low power temperature compensated real time clock (in addition to CPU internal RTC)

DHCS-CPU-Cxxx-Rxxx-EE[-F[P]xxxx][-SPIxx][-RTC][-WBT][-RGB][-PCIe/USB3][-ETH3]-X-01LG	
[-WBT]	WiFi and Bluetooth® via Murata 2FY module with U.FL connector: WBT Note: SDIO1 is no longer available.
[-RGB]	18bit RGB interface is available. Note: UART1 and UART2 are then no longer available.
[-PCIe] or [-USB3]	Either USB3 or PCIe is available on the DHCOS connection.
[-ETH3]	Ethernet port 3 is available on SoC special feature pins of the DHCOS standard. Some GPIOs and I2S are then no longer available.

Table 1: Model number for ordering

Our standard product is defined as follows: **DHCS-STM32MP255C-C120-R409-EE-F1638-SPI04-RTC-WBT-USB3-I-01LG**

Other configurations: On request and please have a look to the product homepage.

4.2.1 RGB variant overview

The STM32MP2x has a limited number of pins. For this reason, the RGB interface is only available if two UART interfaces are not required.

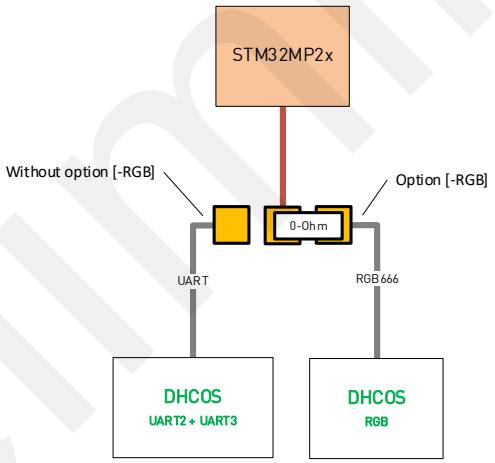


Figure 2: RGB connection

4.2.2 PCIe and USB3 variant overview

The STM32MP2x offers a combo PHY that enables either USB3 Super Speed or PCIe connectivity.

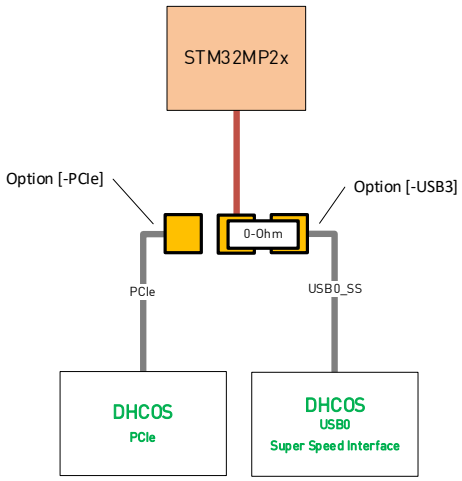


Figure 3: USB3 or PCIe connection

4.2.3 ETH3 variant overview

The STM32MP257 offers a 3rd Ethernet port via the embedded Ethernet switch functionality. The 3rd Ethernet port is only available if I2S, 9x GPIOs and the PCIe_CLKREQ signal can be omitted.

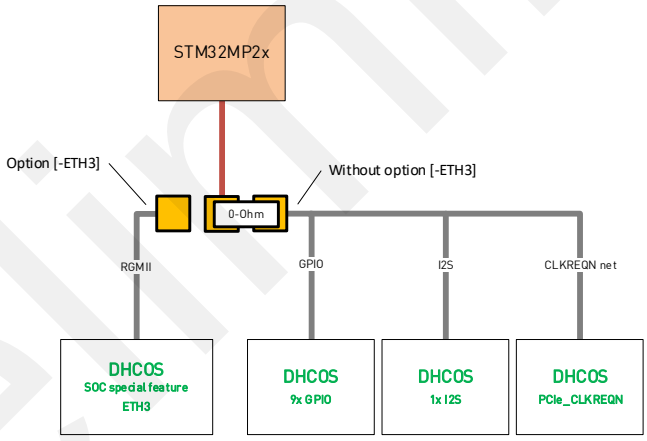


Figure 4: ETH3 connection

4.2.4 WiFi/BT variant overview

The DHCOS STM32MP2x offers WiFi/BT functionality. If WiFi/BT is mounted, the SDIO1 interface is not available.

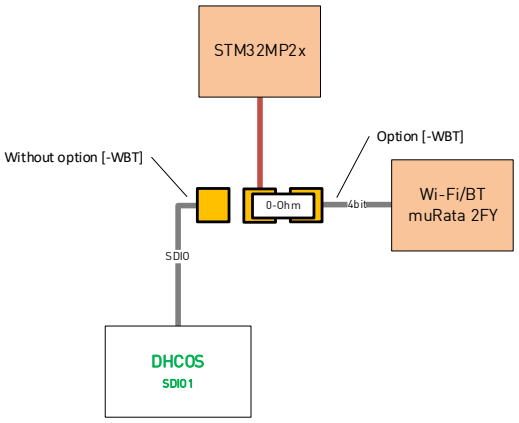


Figure 5: WiFi/BT and SDIO1 connection

4.3 Reference design: DHSBC STM32MP2x (DH Single Board Computer)

The reference design for DHCOS STM32MP2x is the DHSBC STM32MP2x Board:

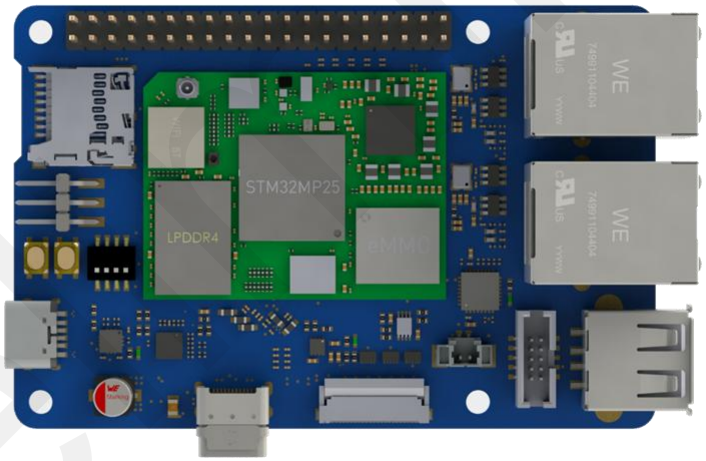


Figure 6: DHSBC STM32MP2x

Important: The DHSBC board is designed to the DHCOS standard. This is not just an evaluation board; it has been designed for harsh industrial use and can be used directly in that environment. It is recommended to transfer parts of this reference design in the own carrier board design, because then the initialization for these parts (Bootloader and Linux Kernel) can then be taken from the DHSBC board, without any BSP porting efforts.

4.3.1 Feature overview

The DHSBC STM32MP2x board provides the following features:

- Based on DHCOS STM32MP2x SOM

- 1x USB 2.0 host port
- 1x USB-C 3.2 Gen 1x1 port with DisplayPort alt. mode support
- 1x USB-C power supply port
- 1x microSD socket
- 2x 1 Gbps Ethernet ports
- 1x LVDS 8-lanes display connector
- 1x Mipi-CSI2 camera connector
- Tri-band WiFi (802.11a/b/g/n/ac/ax) and Bluetooth v5.4 BR/EDR/LE
- Standard Raspberry Pi support
    - 2x CAN
    - 2x I2C
    - 2x UART
    - 1x SPI
    - 2x PWM
    - 1x I2S
    - GPIOs
- Reset button and boot mode switch
- Battery socket for Realtime Clock
- Serial console UART port
- TPM as mounting option
- Industrial product design, CE certified
- 10+ years available

The CubeMx and pin-Mux Files are available here: Links tbd...

4.4 Pin assignment

The DHCOS-STM32MP2-01LG comes with the CPU type STM32MP2xxxAK3 and with 14 x 14 mm VFBGA424 package.

4.4.1 Power supply (input and output)

DHCOS pad name	Description / Notes	Voltage level	DHCOS pad number	Ball Type	I/O Type
VCC_IN	5V supply voltage	5V	A25, A26, A27, A28	PWR	I
GND	GND		A30, A31, B3, B4, B25, B26, B27, C25, C26, C27, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24,	PWR	-

			D25, D26, E9, E25, F9, F25, G9, G25, H9, H25, J9, J25, K9, K25, L9, L25, M9, M25, N9, N25, P9, P25, R9, R25, T9, T25, U9, U25, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, V22, V23, V24, V25, AA3, AA4, AA30, AA31		
VOUT = VIO	IO output voltage → Connected to PMIC: BUCK7	3.3V	B29, C29	PWR	O
VRGMII	RGMII output voltage → Connected to PMIC: BUCK7	3.3V	A29	PWR	O
VSDIO0	SDIO0 output voltage → Connected to PMIC: LDO8	3.3V or 1.8V	C28	PWR	O
VSDIO1	SDIO1 output voltage → Connected to PMIC: BUCK4	3.3V	B28	PWR	O
VRGB	RGB output voltage → Connected to PMIC: BUCK4	3.3V	D27	PWR	O
VRTC	RTC VBACKUP input voltage → Connected to RTC: VBACKUP	1.5V – 3.6V	D28	PWR	I
VBAT	SoC VBAT power domain input voltage	2.6V – 3.6V	D29	PWR	I
ADC_VREF	Analog reference voltage **Note: Must not be connected. Is supplied internally.**	1.1V – 1.8V	F27	PWR	I
SOC_SF5 = VWBT_32k	WiFi/BT 32kHz clock reference voltage 1V8 output voltage → Connected to PMIC: BUCK5	1V8	T8	PWR	O

Table 2: Power supply (input and output)

4.4.2 System signals

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
#PWR_BTN	User power ON key (active low with internal pull-up) → Connected to STPMIC25D pin 1	-	VIO	E26	GPIO	I
PWR_GOOD	Power good output signal. Indicates that PMIC sequencing is complete. (active high)	-	VIO	E27	GPIO	O
#RST_IN	System Reset Input (active low with internal pull-up)	NRST	VIO	E28	GPIO	I
#RST_OUT	System Reset Output (active low with internal pull-up)	-	VIO	E29	GPIO	O
BOOT0	Boot mode pin 0	BOOT0	VIO	F26	Boot	I
BOOT1	Boot mode pin 1	BOOT1	VIO	G26	Boot	I
BOOT2	Boot mode pin 2	BOOT2	VIO	H26	Boot	I
BOOT3	Boot mode pin 3	BOOT3	VIO	J26	Boot	I

Table 3: System signals

4.4.3 JTAG

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
JTAG_TMS	JTAG test mode select	JTMS_SWDIO	VIO	F29	GPIO	I
JTAG_TCK	JTAG test clock	JTCK_SWCLK	VIO	G29	GPIO	I
JTAG_TDI	JTAG test data input	JTDI	VIO	H29	GPIO	I
JTAG_TDO	JTAG test data output	JTDO_TRACESWO	VIO	J29	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
#JTAG_TRST	JTAG test reset (active low)	NJTRST	VIO	K29	GPIO	I

Table 4: JTAG signals

4.4.4 UART / Console

4.4.4.1 UART0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
UART0_TX	UART0 TX transmit data output	PF5	VIO	R29	GPIO	O
UART0_RX	UART0 RX receive data input	PF4	VIO	T29	GPIO	I

Table 5: UART0 / Console

Note: This port is reserved for Linux and bootloader console connection.

4.4.4.2 UART1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
UART1_TX	UART1 TX transmit data output	PB7	VIO	U29	GPIO	O
UART1_RX	UART1 RX receive data input	PB6	VIO	V29	GPIO	I
UART1_RTS	UART1 request to send	PD9	VIO	W28	GPIO	O
UART1_CTS	UART1 clear to send	PD8	VIO	W29	GPIO	I

Table 6: UART1

4.4.4.3 UART2

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
UART2_TX	UART2 TX transmit data output Note: Only available without option -RGB	PG8	VIO	Y28	GPIO	O
UART2_RX	UART2 RX receive data input Note: Only available without option -RGB	PI5	VIO	Y29	GPIO	I
UART2_RTS	UART2 request to send Note: Only available without option -RGB	PF12	VIO	AA28	GPIO	O
UART2_CTS	UART2 clear to send Note: Only available without option -RGB	PG7	VIO	AA29	GPIO	I

Table 7: UART2

4.4.4.4 UART3

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
UART3_TX	UART3 TX transmit data output Note: Only available without option -RGB	PI6	VIO	T27	GPIO	O
UART3_RX	UART3 RX receive data input Note: Only available without option -RGB	PI7	VIO	U27	GPIO	I
UART3_RTS	UART3 request to send Note: Only available without option -RGB	PF14	VIO	W27	GPIO	O
UART3_CTS	UART3 clear to send Note: Only available without option -RGB	PF13	VIO	V27	GPIO	I

Table 8: UART3

4.4.5 SPI

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SPI_SS	SS: slave select pin (active high)	PZ6	VIO	L29	GPIO	O
SPI_SCLK	SCK: serial clock output	PZ5	VIO	M29	GPIO	O
SPI_MISO	MISO: master in / slave out data	PZ8	VIO	N29	GPIO	I
SPI_MOSI	MOSI: master out / slave in data	PZ7	VIO	P29	GPIO	O

Table 9: SPI

4.4.6 QuadSPI

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
QSPI_SS	SS: slave select pin (active high)	PB8	VIO	J8	GPIO	O
QSPI_SCLK	SCK: serial clock output	PB10	VIO	K8	GPIO	O
QSPI_D0	Data bit 0 or SO = MOSI in single-SPI mode	PB0	VIO	L8	GPIO	I/O
QSPI_D1	Data bit 1 or SI = MISO in single-SPI mode	PB1	VIO	M8	GPIO	I/O
QSPI_D2	Data bit 2 or output mode and forced to 0 (to deactivate the "write protect" function) in single-SPI mode	PB2	VIO	N8	GPIO	I/O
QSPI_D3	Data bit 3 or output mode and forced to 1 (to deactivate the "hold" function) in single-SPI mode	PB3	VIO	P8	GPIO	I/O
#QSPI_RST	QSPI reset (active low) → Connected to IO-Expander (I2C: 0x20; P1.4)	-	VIO	R8	GPIO	O

Table 10: QuadSPI

4.4.7 I2C

4.4.7.1 I2C0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2C0_SCL	I²C-bus clock (pull-up on the SOM)	PB5	VIO	E8	GPIO	I/O
I2C0_SDA	I²C-bus data (pull-up on the SOM)	PB4	VIO	F8	GPIO	I/O

Table 11: I2C0

4.4.7.2 I2C1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2C1_SCL	I²C-bus clock (pull-up on the SOM)	PZ4	VIO	G8	GPIO	I/O
I2C1_SDA	I²C-bus data (pull-up on the SOM)	PZ9	VIO	H8	GPIO	I/O

Table 12: I2C1

Note: Some addresses of the DHCOS I2C1 are already pre-assigned on the SOM. Please also have a look at chapter 15 On-Module I2CTM.

4.4.8 GPIO

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
#INT_HIGH_PRIO	General-purpose I/O with wakeup support from deep sleep mode (active low)	PI8	VIO	F28	GPIO	I/O
GPIO_A / DISP_EN	General-purpose I/O / Use as a display enable if your application needs to support this functionality (active high)	PZ2	VIO	G28	GPIO	I/O
GPIO_B / BL_EN	General-purpose I/O / Use as a backlight enable if your application needs to support this functionality (active high)	PZ3	VIO	H28	GPIO	I/O
GPIO_C / #USB_HUB_RST	General-purpose I/O / Use as a USB hub reset line if your application needs to support this functionality (active low)	PI9	VIO	J28	GPIO	I/O
GPIO_D / #USB1_INT	General-purpose I/O / Use as a USB Type-C power delivery controller interrupt line for USB port1, if your application needs to support this functionality (active low)	PA8	VIO	K28	GPIO	I/O
GPIO_E / USB1_SS_SEL	General-purpose I/O / Use as a USB Type-C orientation selection signal for USB port1, if your application needs to support this functionality	PA4	VIO	L28	GPIO	I/O
GPIO_F / USB1_ID	General-purpose I/O / Use as a USB OTG ID line for USB port1, if your application needs to support this functionality	PG14	VIO	M28	GPIO	I/O
GPIO_G	General-purpose I/O Note: Only available without option -ETH3	PH8	VIO	N28	GPIO	I/O
GPIO_H	General-purpose I/O Note: Only available without option -ETH3	PH7	VIO	P28	GPIO	I/O
GPIO_I	General-purpose I/O Note: Only available without option -ETH3	PH2	VIO	R28	GPIO	I/O
GPIO_J	General-purpose I/O Note: Only available without option -ETH3	PA5	VIO	T28	GPIO	I/O
GPIO_K	General-purpose I/O Note: Only available without option -ETH3	PA2	VIO	U28	GPIO	I/O
GPIO_L	General-purpose I/O Note: Only available without option -ETH3	PA3	VIO	V28	GPIO	I/O
GPIO_M	General-purpose I/O Note: Only available without option -ETH3	PA1	VIO	L27	GPIO	I/O
GPIO_N	General-purpose I/O Note: Only available without option -ETH3	PH3	VIO	M27	GPIO	I/O
GPIO_O	General-purpose I/O Note: Only available without option -ETH3	PH6	VIO	N27	GPIO	I/O
GPIO_P	*Not connected with DHCOS STM32MP2*	-	VIO	P27	GPIO	I/O
GPIO_Q	*Not connected with DHCOS STM32MP2*	-	VIO	R27	GPIO	I/O

Table 13: GPIO

Note: It is strongly recommended to use the recommended alternative function of the dedicated pins if your application needs to support the functionality to be as compatible as possible with the DHCOS standard.

4.4.9 I2S

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2S_RXD	RX receive data input	PG1	VIO	K26	GPIO	I
I2S_RXFS	*Not connected with DHCOS STM32MP2*	-	VIO	L26	GPIO	I/O
I2S_RXC	*Not connected with DHCOS STM32MP2*	-	VIO	M26	GPIO	I/O
I2S_TXD	TX transmit data output Note: Only available without option -ETH3	PA10	VIO	N26	GPIO	O
I2S_TXFS	TX frame synchronization line Note: Only available without option -ETH3	PA6	VIO	P26	GPIO	I/O
I2S_TXC	TX audio bit clock Note: Only available without option -ETH3	PA9	VIO	R26	GPIO	I/O

Table 14: I2S

4.4.10 CAN

4.4.10.1 CAN0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
CAN0_TX	CAN transmit pin	PB9	VIO	T26	GPIO	O
CAN0_RX	CAN receive pin	PB11	VIO	U26	GPIO	I

Table 15: CAN0

4.4.10.2 CAN1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
CAN1_TX	CAN transmit pin	PD2	VIO	V26	GPIO	O
CAN1_RX	CAN receive pin	PD1	VIO	W26	GPIO	I

Table 16: CAN1

4.4.11 Analog

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ADC0	Analog input 0	PF3	ADC_VREF	G27	Analog	I
ADC1	Analog input 1	PG2	ADC_VREF	H27	Analog	I
ADC2	*Not connected with DHCOS STM32MP2*	-	ADC_VREF	J27	Analog	I
ADC3	*Not connected with DHCOS STM32MP2*	-	ADC_VREF	K27	Analog	I

Table 17: Analog

4.4.12 PWM

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
PWM0 / BL_PWM	Pulse width modulation output 0 / Use as PWM for backlight dimming, if your application needs to support this functionality	PH4	VIO	A24	GPIO	O
PWM1	Pulse width modulation output 1	PZ1	VIO	B24	GPIO	O
PWM2	*Not connected with DHCOS STM32MP2*	-	VIO	C24	GPIO	O

Table 18: PWM

Note: It is strongly recommended to use the recommended alternative function of the dedicated pins if your application needs to support the functionality to be as compatible as possible with the DHCOS standard.

4.4.13 WiFi/BT

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
WBT_32kHz_REFCLK	External clock input (32.768kHz)	-	VWBT_32k	A6	Clock	I

Table 19: WiFi/BT

4.4.14 Mipi-DSI

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
DSI_CLK+	Differential positive clock	DSI_CKP	D-PHY	W24	DSI	O
DSI_CLK-	Differential negative clock	DSI_CKN	D-PHY	W25	DSI	O
DSI_TX0+	Differential positive data lane 0	DSI_D0P	D-PHY	Y24	DSI	O
DSI_TX0-	Differential negative data lane 0	DSI_D0N	D-PHY	Y25	DSI	O
DSI_TX1+	Differential positive data lane 1	DSI_D1P	D-PHY	AA24	DSI	O
DSI_TX1-	Differential negative data lane 1	DSI_D1N	D-PHY	AA25	DSI	O
DSI_TX2+	Differential positive data lane 2	DSI_D2P	D-PHY	Y26	DSI	O
DSI_TX2-	Differential negative data lane 2	DSI_D2N	D-PHY	Y27	DSI	O
DSI_TX3+	Differential positive data lane 3	DSI_D3P	D-PHY	AA26	DSI	O
DSI_TX3-	Differential negative data lane 3	DSI_D3N	D-PHY	AA27	DSI	O
DSI_TE	DSI panel tearing effect signal	PD15	VIO	Y23	GPIO	I
DISP_EN	*Display enable (active high)*	*PZ2*	*VIO*	*See 4.4.8 GPIO*	*GPIO*	*O*
BL_EN	*Backlight enable (active high)*	*PZ3*	*VIO*		*GPIO*	*O*
BL_PWM	*PWM for backlight dimming*	*PH4*	*VIO*	*See 4.4.12 PWM*	*GPIO*	*O*

Table 20: Mipi-DSI

4.4.15 LVDS

Note: Channel A and B can operate in either single or dual link mode.

4.4.15.1 LVDS0 – channel A

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
LVDS0_CLK+	Differential positive clock	LVDS1_D4P	LVDS	C22	LVDS	O
LVDS0_CLK-	Differential negative clock	LVDS1_D4N	LVDS	C23	LVDS	O
LVDS0_TX0+	Differential positive data lane 0	LVDS1_D0P	LVDS	C20	LVDS	O
LVDS0_TX0-	Differential negative data lane 0	LVDS1_D0N	LVDS	C21	LVDS	O
LVDS0_TX1+	Differential positive data lane 1	LVDS1_D1P	LVDS	C18	LVDS	O
LVDS0_TX1-	Differential negative data lane 1	LVDS1_D1N	LVDS	C19	LVDS	O
LVDS0_TX2+	Differential positive data lane 2	LVDS1_D2P	LVDS	C16	LVDS	O
LVDS0_TX2-	Differential negative data lane 2	LVDS1_D2N	LVDS	C17	LVDS	O
LVDS0_TX3+	Differential positive data lane 3	LVDS1_D3P	LVDS	C14	LVDS	O
LVDS0_TX3-	Differential negative data lane 3	LVDS1_D3N	LVDS	C15	LVDS	O
DISP_EN	*Display enable (active high)*	*PZ2*	*VIO*	*See 4.4.8 GPIO*	*GPIO*	*O*
BL_EN	*Backlight enable (active high)*	*PZ3*	*VIO*		*GPIO*	*O*

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
BL_PWM	*PWM for backlight dimming*	*PH4*	*VIO*	*See 4.4.12 PWM*	*GPIO*	*O*

Table 21: LVDS0 - channel A

4.4.15.2 LVDS1 – channel B

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
LVDS1_CLK+	Differential positive clock	LVDS2_D4P	LVDS	B22	LVDS	O
LVDS1_CLK-	Differential negative clock	LVDS2_D4N	LVDS	B23	LVDS	O
LVDS1_TX0+	Differential positive data lane 0	LVDS2_D0P	LVDS	B20	LVDS	O
LVDS1_TX0-	Differential negative data lane 0	LVDS2_D0N	LVDS	B21	LVDS	O
LVDS1_TX1+	Differential positive data lane 1	LVDS2_D1P	LVDS	B18	LVDS	O
LVDS1_TX1-	Differential negative data lane 1	LVDS2_D1N	LVDS	B19	LVDS	O
LVDS1_TX2+	Differential positive data lane 2	LVDS2_D2P	LVDS	B16	LVDS	O
LVDS1_TX2-	Differential negative data lane 2	LVDS2_D2N	LVDS	B17	LVDS	O
LVDS1_TX3+	Differential positive data lane 3	LVDS2_D3P	LVDS	B14	LVDS	O
LVDS1_TX3-	Differential negative data lane 3	LVDS2_D3N	LVDS	B15	LVDS	O

Table 22: LVDS1 - channel B

4.4.16 Parallel RGB

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
RGB_EN	Data enable Note: Only available with option -RGB	PI5	VRGB	R5	GPIO	O
RGB_VSYNC	Vertical synchronization Note: Only available with option -RGB	PI6	VRGB	P5	GPIO	O
RGB_HSYNC	Horizontal synchronization Note: Only available with option -RGB	PI7	VRGB	M5	GPIO	O
RGB_CLK	Clock output Note: Only available with option -RGB	PF12	VRGB	N5	GPIO	O
RGB_R0	*Not connected with DHCOS STM32MP2*	-	VRGB	E7	GPIO	O
RGB_R1	*Not connected with DHCOS STM32MP2*	-	VRGB	F7	GPIO	O
RGB_R2	Red data bit 2 Note: Only available with option -RGB	PF13	VRGB	G7	GPIO	O
RGB_R3	Red data bit 3 Note: Only available with option -RGB	PF14	VRGB	H7	GPIO	O
RGB_R4	Red data bit 4 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PF15	VRGB	J7	GPIO	O
RGB_R5	Red data bit 5	PG5	VRGB	K7	GPIO	O
RGB_R6	Red data bit 6	PG6	VRGB	L7	GPIO	O
RGB_R7	Red data bit 7 Note: Only available with option -RGB	PG7	VRGB	M7	GPIO	O
RGB_G0	*Not connected with DHCOS STM32MP2*	-	VRGB	E6	GPIO	O
RGB_G1	*Not connected with DHCOS STM32MP2*	-	VRGB	F6	GPIO	O
RGB_G2	Green data bit 2 Note: Only available with option -RGB	PG8	VRGB	G6	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
RGB_G3	Green data bit 3 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PG9	VRGB	H6	GPIO	O
RGB_G4	Green data bit 4 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PG10	VRGB	J6	GPIO	O
RGB_G5	Green data bit 5	PG11	VRGB	K6	GPIO	O
RGB_G6	Green data bit 6	PG12	VRGB	L6	GPIO	O
RGB_G7	Green data bit 7	PG13	VRGB	M6	GPIO	O
RGB_B0	*Not connected with DHCOS STM32MP2*	-	VRGB	D5	GPIO	O
RGB_B1	*Not connected with DHCOS STM32MP2*	-	VRGB	E5	GPIO	O
RGB_B2	Blue data bit 2 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PG15	VRGB	F5	GPIO	O
RGB_B3	Blue data bit 3 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PI0	VRGB	G5	GPIO	O
RGB_B4	Blue data bit 4 Note: Used for coding on the SOM. 10k PU or PD connected on the SOM.	PI1	VRGB	H5	GPIO	O
RGB_B5	Blue data bit 5	PI2	VRGB	J5	GPIO	O
RGB_B6	Blue data bit 6	PI3	VRGB	K5	GPIO	O
RGB_B7	Blue data bit 7	PI4	VRGB	L5	GPIO	O
DISP_EN	*Display enable (active high)*	*PZ2*	*VIO*	*See 4.4.8 GPIO*	*GPIO*	*O*
BL_EN	*Backlight enable (active high)*	*PZ3*	*VIO*		*GPIO*	*O*
BL_PWM	*PWM for backlight dimming*	*PH4*	*VIO*	*See 4.4.12 PWM*	*GPIO*	*O*

Table 23: Parallel RGB

4.4.17 DisplayPort / HDMI

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
DPAUX+	*Not connected with DHCOS STM32MP2*	-	DP	B30	DP	I/O
DPAUX-	*Not connected with DHCOS STM32MP2*	-	DP	C30	DP	I/O
DP0+/HDMI_D0+	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	D30	DP/HDMI	O
DP0-/HDMI_D0-	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	E30	DP/HDMI	O
DP1+/HDMI_D1+	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	F30	DP/HDMI	O
DP1-/HDMI_D1-	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	G30	DP/HDMI	O
DP2+/HDMI_D2+	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	H30	DP/HDMI	O
DP2-/HDMI_D2-	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	J30	DP/HDMI	O
DP3+/HDMI_CLK+	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	K30	DP/HDMI	O
DP3-/HDMI_CLK-	*Not connected with DHCOS STM32MP2*	-	DP/HDMI	L30	DP/HDMI	O
DP_HPD/HDMI_HPD	*Not connected with DHCOS STM32MP2*	-	VIO	M30	GPIO	I
HDMI_CEC	*Not connected with DHCOS STM32MP2*	-	VIO	N30	GPIO	I/O

Table 24: DisplayPort / HDMI

4.4.18 Mipi-CSI2

4.4.18.1 CSI0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
CSI0_CLK+	Differential positive clock	CSI_CKP	D-PHY	W14	CSI	I
CSI0_CLK-	Differential negative clock	CSI_CKN	D-PHY	W15	CSI	I
CSI0_TX0+	Differential positive data lane 0	CSI_D0P	D-PHY	W16	CSI	I
CSI0_TX0-	Differential negative data lane 0	CSI_D0N	D-PHY	W17	CSI	I
CSI0_TX1+	Differential positive data lane 1	CSI_D1P	D-PHY	W18	CSI	I
CSI0_TX1-	Differential negative data lane 1	CSI_D1N	D-PHY	W19	CSI	I
CSI0_TX2+	*Not connected with DHCOS STM32MP2*	-	D-PHY	W20	CSI	I
CSI0_TX2-	*Not connected with DHCOS STM32MP2*	-	D-PHY	W21	CSI	I
CSI0_TX3+	*Not connected with DHCOS STM32MP2*	-	D-PHY	W22	CSI	I
CSI0_TX3-	*Not connected with DHCOS STM32MP2*	-	D-PHY	W23	CSI	I
#CSI0_PWDN	Camera 0 power down pin (0 = power down / 1 = active) → Connected to IO-Expander (I2C: 0x20; P1.5)	-	VIO	W12	GPIO	O
#CSI0_RST	Camera 0 reset (active low) → Connected to IO-Expander (I2C: 0x20; P1.6)	-	VIO	W13	GPIO	O

Table 25: Mipi-CSI2 port 0

4.4.18.2 CSI1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
CSI1_CLK+	*Not connected with DHCOS STM32MP2*	-	D-PHY	L4	CSI	I
CSI1_CLK-	*Not connected with DHCOS STM32MP2*	-	D-PHY	M4	CSI	I
CSI1_TX0+	*Not connected with DHCOS STM32MP2*	-	D-PHY	J4	CSI	I
CSI1_TX0-	*Not connected with DHCOS STM32MP2*	-	D-PHY	K4	CSI	I
CSI1_TX1+	*Not connected with DHCOS STM32MP2*	-	D-PHY	G4	CSI	I
CSI1_TX1-	*Not connected with DHCOS STM32MP2*	-	D-PHY	H4	CSI	I
CSI1_TX2+	*Not connected with DHCOS STM32MP2*	-	D-PHY	E4	CSI	I
CSI1_TX2-	*Not connected with DHCOS STM32MP2*	-	D-PHY	F4	CSI	I
CSI1_TX3+	*Not connected with DHCOS STM32MP2*	-	D-PHY	C4	CSI	I
CSI1_TX3-	*Not connected with DHCOS STM32MP2*	-	D-PHY	D4	CSI	I
#CSI1_PWDN	*Not connected with DHCOS STM32MP2*	-	VIO	P4	GPIO	O
#CSI1_RST	*Not connected with DHCOS STM32MP2*	-	VIO	N4	GPIO	O

Table 26: Mipi-CSI2 port 1

4.4.19 Ethernet

Note: Both ports support RGMII and RMII mode to provide a 1 Gbps or 100 Mbps Ethernet interface.

4.4.19.1 ETH0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ETH0_TX_CTL	Multiplexing of transmitter enable and transmitter error	PA13	VRGMII	A7	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
	(RMII mode = RMII_TX_EN)					
ETH0_TD0	Transmit data bit 0	PA15	VRGMII	A11	GPIO	O
ETH0_TD1	Transmit data bit 1	PC1	VRGMII	A10	GPIO	O
ETH0_TD2	Transmit data bit 2	PH10	VRGMII	A9	GPIO	O
ETH0_TD3	Transmit data bit 3	PH11	VRGMII	A8	GPIO	O
ETH0_TXC	Transmit clock	PC0	VRGMII	A12	GPIO	O
ETH0_RX_CTL	Multiplexing of data received is valid and receiver error (RMII mode = RMII_CRS_DV)	PA11	VRGMII	A13	GPIO	I
ETH0_RD0	Receive data bit 0	PF1	VRGMII	A17	GPIO	I
ETH0_RD1	Receive data bit 1	PC2	VRGMII	A16	GPIO	I
ETH0_RD2	Receive data bit 2	PH12	VRGMII	A15	GPIO	I
ETH0_RD3	Receive data bit 3	PH13	VRGMII	A14	GPIO	I
ETH0_RXC	RGMII Receive clock	PA14	VRGMII	A18	GPIO	I
#ETH0_RST	Ethernet PHY reset (active low) → Connected to IO-Expander (I2C: 0x20; P0.1)	-	VIO	A19	GPIO	O
ETH0_INT	Ethernet PHY interrupt (active high)	PC6	VIO	A20	GPIO	I
ETH0_REFCLK	RGMII reference clock (=125 MHz) (optional)	PH9	VRGMII	A21	GPIO	I
ETH0_MDIO	Management bus data signal	PF2	VRGMII	A22	GPIO	I/O
ETH0_MDC	Management bus clock signal	PF0	VRGMII	A23	GPIO	O

Table 27: Ethernet Port 0

4.4.19.2 ETH1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ETH1_TX_CTL	Multiplexing of transmitter enable and transmitter error (RMII mode = RMII_TX_EN)	PC4	VRGMII	AA7	GPIO	O
ETH1_TD0	Transmit data bit 0	PC7	VRGMII	AA11	GPIO	O
ETH1_TD1	Transmit data bit 1	PC8	VRGMII	AA10	GPIO	O
ETH1_TD2	Transmit data bit 2	PC9	VRGMII	AA9	GPIO	O
ETH1_TD3	Transmit data bit 3	PC10	VRGMII	AA8	GPIO	O
ETH1_TXC	Transmit clock	PF7	VRGMII	AA12	GPIO	O
ETH1_RX_CTL	Multiplexing of data received is valid and receiver error (RMII mode = RMII_CRS_DV)	PC3	VRGMII	AA13	GPIO	I
ETH1_RD0	Receive data bit 0	PG0	VRGMII	AA17	GPIO	I
ETH1_RD1	Receive data bit 1	PC12	VRGMII	AA16	GPIO	I
ETH1_RD2	Receive data bit 2	PF9	VRGMII	AA15	GPIO	I
ETH1_RD3	Receive data bit 3	PC11	VRGMII	AA14	GPIO	I
ETH1_RXC	RGMII Receive clock	PF6	VRGMII	AA18	GPIO	I
#ETH1_RST	Ethernet PHY reset (active low) → Connected to IO-Expander (I2C: 0x20; P0.0)	-	VIO	AA19	GPIO	O
ETH1_INT	Ethernet PHY interrupt (active high)	PG3	VIO	AA20	GPIO	I
ETH1_REFCLK	RGMII reference clock (=125 MHz) (optional)	PF8	VRGMII	AA21	GPIO	I
ETH1_MDIO	Management bus data signal	PC5	VRGMII	AA22	GPIO	I/O
ETH1_MDC	Management bus clock signal	PG4	VRGMII	AA23	GPIO	O

Table 28: Ethernet Port 1

4.4.20 USB

4.4.20.1 USB0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
USB0_VBUS	USB VBUS power detection Note: Connection to PF10 via voltage divider!!!	PF10	20V	D8	PWR	I
USB0_PWR_EN	Enable signal for the bus voltage output in host mode (active high) → Connected to IO-Expander (I2C: 0x20; P0.6)	-	VIO	B9	GPIO	O
#USB0_PWR_STAT	Overcurrent input signal (active low) → Connected to IO-Expander (I2C: 0x20; P0.7)	-	VIO	C9	GPIO	I
USB0_ID	USB OTG ID line Note: USB0_ID is shorted with #USB0_INT	PZ0	VIO	B10	GPIO	I
#USB0_INT	USB Type-C power delivery controller interrupt line (active low) Note: #USB0_INT is shorted with USB0_ID	PZ0	VIO	C10	GPIO	I
USB0_SS_SEL	USB Type-C orientation selection signal External selection: ▪ Low = CC2 orientation ▪ High = CC1 orientation → Connected to IO-Expander (I2C: 0x20; P1.1)	-	VIO	D7	GPIO	O
USB0_D+	USB 2.0 differential positive data lane	USB3DR_DP	USB	C11	USB	I/O
USB0_D-	USB 2.0 differential negative data lane	USB3DR_DM	USB	B11	USB	I/O
USB0_SS_TX+	USB 3.x positive differential transmission signal Note: Only available with option -USB3	COMBO-PHY_TX1P	USB	B12	USB	O
USB0_SS_TX-	USB 3.x negative differential transmission signal Note: Only available with option -USB3	COMBO-PHY_TX1N	USB	B13	USB	O
USB0_SS_RX+	USB 3.x positive differential receiving signal Note: Only available with option -USB3	COMBO-PHY_RX1P	USB	C12	USB	I
USB0_SS_RX-	USB 3.x negative differential receiving signal Note: Only available with option -USB3	COMBO-PHY_RX1N	USB	C13	USB	I

Table 29: USB0

4.4.20.2 USB1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
USB1_VBUS	USB VBUS power detection	-	20V	D6	PWR	I
USB1_PWR_EN	Enable signal for the bus voltage output in host mode (active high) → Connected to IO-Expander (I2C: 0x20; P0.4)	-	VIO	B5	GPIO	O
#USB1_PWR_STAT	Overcurrent input signal (active low) → Connected to IO-Expander (I2C: 0x20; P0.5)	-	VIO	C5	GPIO	I
USB1_ID	*USB OTG ID line*	*PG14*	*VIO*	*See 4.4.8 GPIO*	*GPIO*	*I*
#USB1_INT	*USB Type-C power delivery controller interrupt line (active low)*	*PA8*	*VIO*		*GPIO*	*I*
USB1_SS_SEL	*USB Type-C orientation selection signal* *External selection:*	*PA4*	*VIO*		*GPIO*	*O*

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
	▪ *Low = CC2 orientation* ▪ *High = CC1 orientation*					
USB1_D+	USB 2.0 differential positive data lane	USBH_HS_DP	USB	C6	USB	I/O
USB1_D-	USB 2.0 differential negative data lane	USBH_HS_DM	USB	B6	USB	I/O
USB1_SS_TX+	*Not connected with DHCOS STM32MP2*	-	USB	B7	USB	O
USB1_SS_TX-	*Not connected with DHCOS STM32MP2*	-	USB	B8	USB	O
USB1_SS_RX+	*Not connected with DHCOS STM32MP2*	-	USB	C7	USB	I
USB1_SS_RX-	*Not connected with DHCOS STM32MP2*	-	USB	C8	USB	I

Table 30: USB1

Note: USB port1 does not support Type-C control lines by default, but selected GPIOs can be used to support this feature.

4.4.21 PCIe

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
#PCIe_RST	Dedicated PCIe reset output (active low) → Connected to IO-Expander (I2C: 0x20; P1.2)	-	VIO	V5	GPIO	O
#PCIe_CLKREQ	PCIe reference clock request (active low, pull-up on the SOM) Notes: ▪ Open drain output of the PCIe card. ▪ The SOM can activate an external PCIe clock generator output via I2C after detecting a low signal on this line. Note: Only available without option -ETH3	PA7	VIO	W5	GPIO	I
#PCIe_Wake	Host wakeup signal (active low) → Connected to IO-Expander (I2C: 0x20; P1.3)	-	VIO	V8	GPIO	I
PCIe_CLK_IN+	PCIe 100MHz positive reference clock input	PCIE_CLKINP	PCIe	W6	PCIe	I
PCIe_CLK_IN-	PCIe 100MHz negative reference clock input	PCIE_CLKINN	PCIe	W7	PCIe	I
PCIe_RX+	PCIe positive receive data signal Note: Only available with option -PCIe	COMBO-PHY_RX1P	PCIe	W8	PCIe	I
PCIe_RX-	PCIe negative receive data signal Note: Only available with option -PCIe	COMBO-PHY_RX1N	PCIe	W9	PCIe	I
PCIe_TX+	PCIe positive transmit data signal Note: Only available with option -PCIe	COMBO-PHY_TX1P	PCIe	W10	PCIe	O
PCIe_TX-	PCIe negative transmit data signal Note: Only available with option -PCIe	COMBO-PHY_TX1N	PCIe	W11	PCIe	O

Table 31: PCIe

4.4.22 SDIO

4.4.22.1 SDIO0

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SDIO0_CD	Card detect (active high) → Connected to IO-Expander (I2C: 0x20; P1.0)	-	VIO	T5	GPIO	I
SDIO0_CLK	Clock output	PE3	VSDIO0	N6	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SDIO0_CMD	Command signal	PE2	VSDIO0	P6	GPIO	I/O
SDIO0_D0	Data signal bit 0	PE4	VSDIO0	R6	GPIO	I/O
SDIO0_D1	Data signal bit 1	PE5	VSDIO0	T6	GPIO	I/O
SDIO0_D2	Data signal bit 2	PE0	VSDIO0	U6	GPIO	I/O
SDIO0_D3	Data signal bit 3	PE1	VSDIO0	V6	GPIO	I/O

Table 32: SDIO0

4.4.22.2 SDIO1

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SDIO1_CD	Card detect (active high) → Connected to IO-Expander (I2C: 0x20; P0.3) Note: Only available without option -WBT	-	VIO	U5	GPIO	I
SDIO1_CLK	Clock output Note: Only available without option -WBT	PB13	VSDIO1	N7	GPIO	O
SDIO1_CMD	Command signal Note: Only available without option -WBT	PD12	VSDIO1	P7	GPIO	I/O
SDIO1_D0	Data signal bit 0 Note: Only available without option -WBT	PB14	VSDIO1	R7	GPIO	I/O
SDIO1_D1	Data signal bit 1 Note: Only available without option -WBT	PD13	VSDIO1	T7	GPIO	I/O
SDIO1_D2	Data signal bit 2 Note: Only available without option -WBT	PB12	VSDIO1	U7	GPIO	I/O
SDIO1_D3	Data signal bit 3 Note: Only available without option -WBT	PD14	VSDIO1	V7	GPIO	I/O

Table 33: SDIO1

4.4.23 SoC special feature

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SOC_SF0	PCIe_CLKOUTN PCIe 100MHz negative reference clock output	PCIE_CLKIOUTN	PCIe	Y5	PCIe	O
SOC_SF1	USB1_CC1 USB Type-C® Power Delivery control CC1 line	UCPD1_CC1	USBC	AA5	Analog	I/O
SOC_SF2	PCIe_CLKOUTP PCIe 100MHz positive reference clock input	PCIE_CLKIOUTP	PCIe	Y6	PCIe	O
SOC_SF3	USB1_CC2 USB Type-C® Power Delivery control CC2 line	UCPD1_CC2	USBC	AA6	Analog	I/O
SOC_SF4	ETH3_TX_CTL Multiplexing of transmitter enable and transmitter error (RMII mode = RMII_TX_EN)	PA3	VIO	Y7	GPIO	O
SOC_SF5	1V8 output voltage → Connected to PMIC: BUCK5	-	1V8	T8	PWR	O
SOC_SF6	RTC_EVI RTC event input → Connected to RV-3032-C7 EVI pin 4 Note: Only available with option -RTC	-	VIO	U8	GPIO	I
SOC_SF7	ETH3_TD3	PH3	VIO	Y8	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
	Transmit data bit 3 Note: Only available with option -ETH3					
SOC_SF8	ETH3_TD2 Transmit data bit 2 Note: Only available with option -ETH3	PH6	VIO	Y9	GPIO	O
SOC_SF9	ETH3_TD1 Transmit data bit 1 Note: Only available with option -ETH3	PA7	VIO	Y10	GPIO	O
SOC_SF10	ETH3_TD1 Transmit data bit 0 Note: Only available with option -ETH3	PA6	VIO	Y11	GPIO	O
SOC_SF11	ETH3_TXC Transmit clock Note: Only available with option -ETH3	PH2	VIO	Y12	GPIO	O
SOC_SF12	ETH3_RX_CTL Multiplexing of data received is valid and receiver error (RMII mode = RMII_CRS_DV) Note: Only available with option -ETH3	PA2	VIO	Y13	GPIO	I
SOC_SF13	ETH3_RD3 Receive data bit 3 Note: Only available with option -ETH3	PH8	VIO	Y14	GPIO	I
SOC_SF14	ETH3_RD2 Receive data bit 2 Note: Only available with option -ETH3	PH7	VIO	Y15	GPIO	I
SOC_SF15	ETH3_RD1 Receive data bit 1 Note: Only available with option -ETH3	PA10	VIO	Y16	GPIO	I
SOC_SF16	ETH3_RD0 Receive data bit 0 Note: Only available with option -ETH3	PA9	VIO	Y17	GPIO	I
SOC_SF17	ETH3_RXC Receive clock Note: Only available with option -ETH3	PA5	VIO	Y18	GPIO	I
SOC_SF18	#ETH3_RST Ethernet PHY reset (active low) → Connected to IO-Expander (I2C: 0x20; P1.7)	-	VIO	Y19	GPIO	O
SOC_SF19	ETH3_INT Ethernet PHY interrupt (active high) Note: Only available with option -ETH3	PA1	VIO	Y20	GPIO	I
SOC_SF20	WL_HOST_WAKE WiFi host wake output → Connected to muRata 2FY pin 2 (GPIO_0/WL_HOST_WAKE) Note: Only available with option -WBT	-	1V8	Y21	GPIO	O
SOC_SF21	BT_HOST_WAKE Bluetooth host wake output → Connected to muRata 2FY pin 41 (BT_HOST_WAKE) Note: Only available with option -WBT	-	1V8	Y22	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SOC_SF22	WL_DEV_WAKE WiFi device wake input → Connected to muRata 2FY pin 5 (GPIO_1/ LHL) Note: Only available with option -WBT	-	1V8	R4	GPIO	I
SOC_SF23	*Not connected with DHCOS STM32MP2*	-	-	T4	-	-
SOC_SF24	*Not connected with DHCOS STM32MP2*	-	-	U4	-	-
SOC_SF25	*Not connected with DHCOS STM32MP2*	-	-	V4	-	-
SOC_SF26	*Not connected with DHCOS STM32MP2*	-	-	W4	-	-
SOC_SF27	*Not connected with DHCOS STM32MP2*	-	-	Y4	-	-
SOC_SF28	*Not connected with DHCOS STM32MP2*	-	-	P30	-	-
SOC_SF29	*Not connected with DHCOS STM32MP2*	-	-	R30	-	-
SOC_SF30	*Not connected with DHCOS STM32MP2*	-	-	T30	-	-
SOC_SF31	*Not connected with DHCOS STM32MP2*	-	-	U30	-	-
SOC_SF32	*Not connected with DHCOS STM32MP2*	-	-	V30	-	-
SOC_SF33	*Not connected with DHCOS STM32MP2*	-	-	W30	-	-
SOC_SF34	*Not connected with DHCOS STM32MP2*	-	-	Y30	-	-

Table 34: SoC special feature pins

4.5 Mandatory connections

The pins listed in the following table must be connected. Any other connections that are not required may remain open.

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
VCC_IN	5V supply voltage	-	5V	A25, A26, A27, A28	PWR	I
GND	GND	-		A30, A31, B3, B4, B25, B26, B27, C25, C26, C27, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, E9, E25, F9, F25, G9, G25, H9, H25, J9, J25, K9, K25, L9, L25, M9, M25, N9, N25, P9, P25, R9, R25, T9, T25, U9, U25, V9, V10, V11, V12, V13, V14,	PWR	-

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
				V15, V16, V17, V18, V19, V20, V21, V22, V23, V24, V25, AA3, AA4, AA30, AA31		
BOOT0	Boot mode pin 0	BOOT0	VIO	F26	Boot	I
BOOT1	Boot mode pin 1	BOOT1	VIO	G26	Boot	I
BOOT2	Boot mode pin 2	BOOT2	VIO	H26	Boot	I
BOOT3	Boot mode pin 3	BOOT3	VIO	J26	Boot	I
UART0_TX	UART0 TX transmit data output	PF5	VIO	R29	GPIO	O
UART0_RX	UART0 RX receive data input	PF4	VIO	T29	GPIO	I
USB0_D+	USB 2.0 differential positive data lane	USB3DR_DP	USB	C11	USB	I/O
USB0_D-	USB 2.0 differential negative data lane	USB3DR_DM	USB	B11	USB	I/O
WBT_32kHz_REFCLK	External clock input (32.768kHz) **Note: Only needed for DHCOS with WiFi/BT**	-	VWBT_32k	A6	Clock	I

Table 35: Mandatory connections

Notes:

- UART0 is required to provide a serial connection for the bootloader and the Linux console.
- BOOT mode pins must be configured by the mainboard design to select the correct boot device.
- USB0 is required to support USB boot for board bring-up.

5 Protection circuits

The DHCOS-STM32MP2-01LG module does **NOT** contain any protection circuits (e.g. ESD protection). These must be provided from the carrier board.

6 Power supply

The DHCOS-STM32MP2-01LG must be powered by a single 5.0 V supply voltage on the VCC_IN pins. All other voltages are directly generated by the STPMIC25D and can also be used on the carrier board for the supply of peripheral components (Ethernet PHY, eMMC, ...). This enables a carrier board design with only one buck regulator for the 5.0 V DHCOS supply voltage.

Note: The power supply must be buffered with at least two 47uF capacitors on the carrier board.

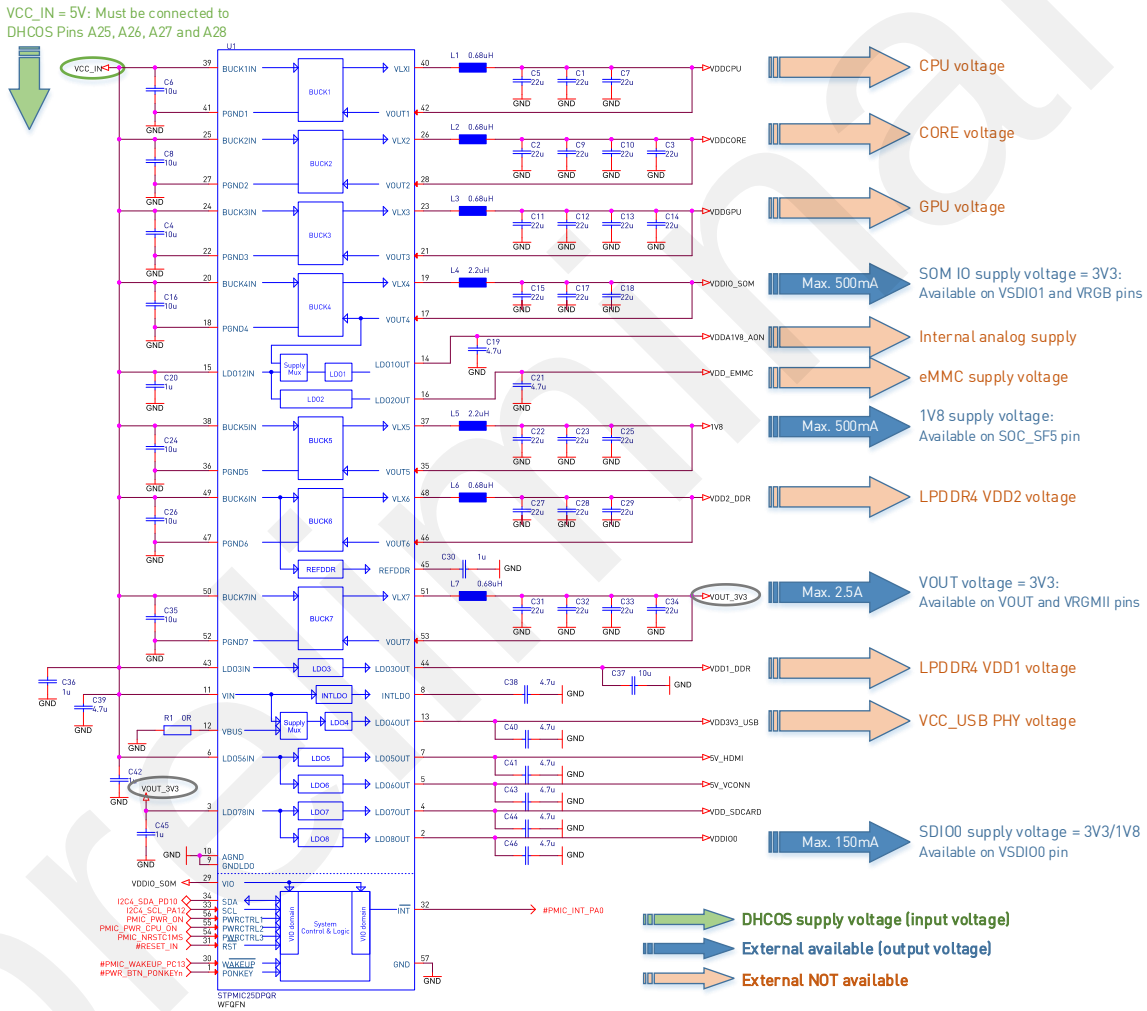


Figure 7: Power supply overview

Notes:

- When designing a carrier board, the EMC performance can be improved by adding filters to the supply voltages of the DHCOS module.

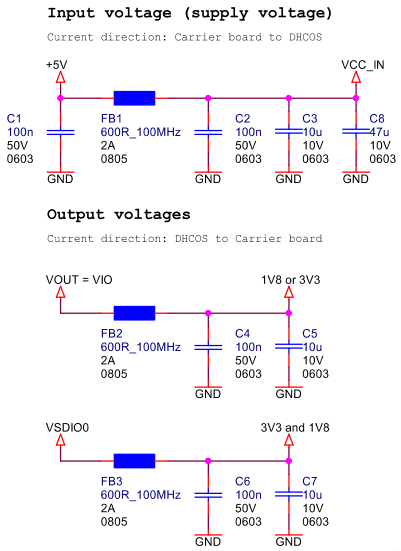


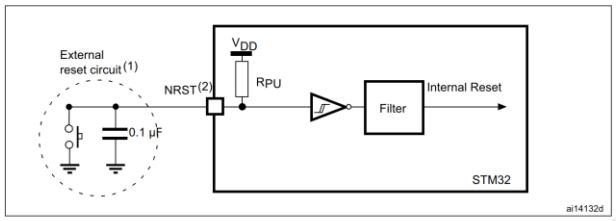
Figure 8: Power supply filtering

Filtering notes:

- Recommended ferrite: Wuerth 742792040 (maximum current of any supply voltage must be checked) or similar

7 Reset

The reset signal #RST_IN is active low and directly connected to the STM32MP2x NRST and PMIC RST pin. VDD is connected to VOUT = VIO voltage.



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST/NRST_CORE pin can go below the $V_{IL(NRST)}$ max level

Figure 9: Reset

Notes: The 0.1µF capacitor is necessary, even if #RST_IN is not used on the carrier board. It is also recommended to trigger a reset event (from the carrier board) only via an open-drain circuit. Do not connect NRST directly to VIO.

For more precise technical information, we refer you to the ST reset documentation.

The signal #RST_OUT reflects the state of #RST_IN but is decoupled from it.

8 Boot modes

The STM32MP2 BOOT pins are directly available on the DHCOS pins F26, G26, H26 and J26. No pull-up or pull-down resistors are added to the BOOT pins at the DHCOS module. These parts **MUST** be added external on the carrier board.

The default boot device is the Serial NOR-Flash on the System on Module. Alternatively, SOM variants are available with only the eMMC mounted. Depending on the SOM used, the customer must ensure that the boot pin settings on the carrier board are correct, or the OTP settings must be changed.

BOOT3	BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	0	UART and USB	Wait incoming connection on: – USART6 = DHCOS UART0 – USB high-speed device on USB3DR_DP/DM = DHCOS USB0
0	**0**	**0**	**1**	**SD card**	SDMMC1 = DHCOS SDIO0
0	**0**	**1**	**0**	**eMMC**	SDMMC2 = eMMC located on System-On-Module
0	0	1	1	Development boot (no flash boot)	Used to get debug access without boot from flash memory
0	**1**	**0**	**0**	**Serial NOR-Flash**	OCTOSPIM_P1 = Quad SPI located on System-On-Module
For all other boot mode options, please refer to the STM32MP2 datasheet.					

Table 36: Boot modes

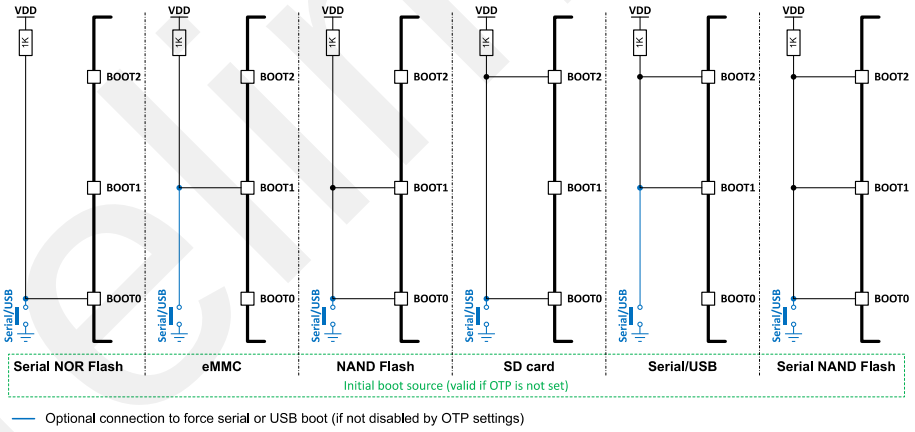


Figure 10: Typical connection schematics of BOOT pins

8.1 SD card boot

Note: SD card boot is only available on DHCOS SDIO0 interface.

If the carrier board contains a microSD/SD socket and it is planned to boot form microSD/SD card, it is mandatory to connect the card at the following CPU pins (otherwise SD-Card boot will not work):

- PE3: SDMMC1_CK = DHCOS SDIO0_CLK
- PE2: SDMMC1_CMD = DHCOS SDIO0_CMD
- PE4: SDMMC1_D0 = DHCOS SDIO0_D0

Please also have a look at the ST application note AN5489 "**Getting started with STM32MP25x MPUs hardware development**".

9 IO-Expander

On the DHCOS-STM32MP2-01LG some slower IO signals are realized via an IO-expander, as there are not enough free native GPIOs available on the STM32MP2. The Kinetic KTS1622EUAA IO-Expander is connected to the MP2 I2C8. This interface is also connected to the DHCOS I2C1. Please also have a look at chapter 15 On-Module I2CTM

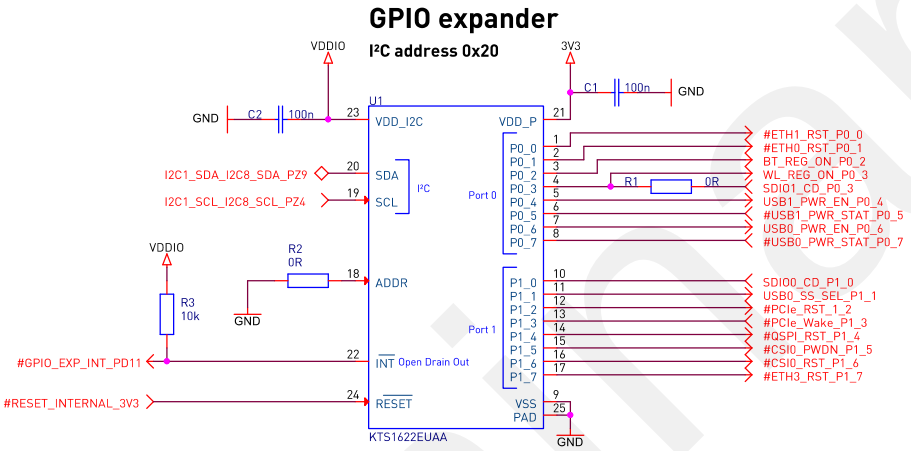


Figure 11: IO-Expander

DHCOS pad name	Description / Notes	IO expander pin	Voltage level	DHCOS pad number	Ball Type	I/O Type
#ETH1_RST	Ethernet PHY reset (active low)	P0.0	VIO	AA19	GPIO	O
#ETH0_RST	Ethernet PHY reset (active low)	P0.1	VIO	A19	GPIO	O
BT_REG_ON	Bluetooth muRata 2FY power on GPIO: Used by the PMU to power up or power down the internal CYW55513 regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pulldown resistor that is auto enabled/disabled by programming.	P0.2	VIO	-	GPIO	O
WL_REG_ON	WiFi muRata 2FY power on GPIO: Used by the PMU to power up or power down the internal CYW55513 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 KΩ pull down resistor that is auto enabled/disabled by programming. Note: Only use as WL_REG_ON with option -WBT	P0.3	VIO	-	GPIO	O
SDIO1_CD	Card detect (active high) Notes: ▪ Only available without option -WBT ▪ R1 is only mounted without option -WBT	P0.3	VIO	U5	GPIO	I

DHCOS pad name	Description / Notes	IO expander pin	Voltage level	DHCOS pad number	Ball Type	I/O Type
USB1_PWR_EN	Enable signal for the bus voltage output in host mode (active high)	P0.4	VIO	B5	GPIO	O
#USB1_PWR_STAT	Overcurrent input signal (active low)	P0.5	VIO	C5	GPIO	I
USB0_PWR_EN	Enable signal for the bus voltage output in host mode (active high)	P0.6	VIO	B9	GPIO	O
#USB0_PWR_STAT	Overcurrent input signal (active low)	P0.7	VIO	C9	GPIO	I
SDIO0_CD	Card detect (active high)	P1.0	VIO	T5	GPIO	I
USB0_SS_SEL	USB Type-C orientation selection signal External selection: ▪ Low = CC2 orientation ▪ High = CC1 orientation	P1.1	VIO	D7	GPIO	O
#PCIe_RST	Dedicated PCIe reset output (active low)	P1.2	VIO	V5	GPIO	O
#PCIe_Wake	Host wakeup signal (active low)	P1.3	VIO	V8	GPIO	I
#QSPI_RST	QSPI reset (active low)	P1.4	VIO	R8	GPIO	O
#CSI0_PWDN	Camera 0 power down pin (0 = power down / 1 = active)	P1.5	VIO	W12	GPIO	O
#CSI0_RST	Camera 0 reset (active low)	P1.6	VIO	W13	GPIO	O
SOC_SF18	#ETH3_RST Ethernet PHY reset (active low)	P1.7	VIO	Y19	GPIO	O

Table 37: IO-Expander

10 eMMC flash memory

As non-volatile data storage, the DHCOS-STM32MP2-01LG module provides an eMMC flash memory to store the bootloader, operating system and application data on it. However, as a DH standard, the bootloader is stored in the Quad SPI NOR-Flash (see 11 Quad SPI NOR-Flash).

The eMMC is connected to the 8-bit SDMMC2 interface of the STM32MP2 SoC. The size of the eMMC starts from 4 GByte and depends on the ordering configuration.

The DHCOS-STM32MP2-01LG supports the HS200 operating mode as maximum interface speed.

Note: eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly.

Please have a look at: https://en.wikipedia.org/wiki/Flash_memory#Write_endurance

In order to increase the maximum number of eMMC write and erase cycles, DH electronics also offers the possibility to mount pSLC (pseudo SLC) eMMC memory. pSLC is a configuration of the MLC NAND flash memory that uses half the cell capacity - i.e. 1 bit per cell instead of 2 bits per cell - to improve the reliability, performance and endurance of the eMMC.

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SDMMC2_CK	Clock output	PE14	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_CMD	Command signal	PE15	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D0	Data signal bit 0	PE13	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D1	Data signal bit 1	PE11	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D2	Data signal bit 2	PE8	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D3	Data signal bit 3	PE12	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D4	Data signal bit 4	PE10	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D5	Data signal bit 5	PE9	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D6	Data signal bit 6	PE6	VDD_EMMC = PMIC LDO2	-	GPIO	I/O
SDMMC2_D7	Data signal bit 7	PE7	VDD_EMMC = PMIC LDO2	-	GPIO	I/O

Table 38: eMMC

Note: The listed STM32MP2 pins are not available externally, although no eMMC is mounted on the SOM.

11 Quad SPI NOR-Flash

The onboard Quad SPI NOR-Flash is connected to the OCTOSPIM interface port 1 of the STM32MP2. By default, the bootloader is stored in SPI NOR-Flash and the Linux Image is located in eMMC flash. Therefore, the boot mode must be set by default to Serial NOR-Flash boot (see also 8 Boot modes).

It is possible to order the DHCOS module without onboard Quad SPI NOR-Flash as well (without option -SPIxx). Then the bootloader must be stored in eMMC flash memory and the boot mode must be set to eMMC boot (see also 8 Boot modes).

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
OCTOSPIM_P1_CLK	OCTOSPI clock	PD0	VIO	-	GPIO	I/O
OCTOSPIM_P1_NCS1	Chip select for the memory	PD3	VIO	-	GPIO	I/O
OCTOSPIM_P1_IO0	OCTOSPI Data pin 0	PD4	VIO	-	GPIO	I/O
OCTOSPIM_P1_IO1	OCTOSPI Data pin 1	PD5	VIO	-	GPIO	I/O
OCTOSPIM_P1_IO2	OCTOSPI Data pin 2	PD6	VIO	-	GPIO	I/O
OCTOSPIM_P1_IO3	OCTOSPI Data pin 3	PD7	VIO	-	GPIO	I/O

Table 39: Quad SPI NOR-Flash

Note: The listed STM32MP2 pins are not available externally, although no SPI NOR-Flash is mounted on the SOM.

12 EEPROM

The DHCOS-STM32MP2-01LG comes with additional 256 kbit onboard EEPROM M24256E from ST. It is connected to the STM32MP2 I2C8 port. Please also have a look at chapter 15 On-Module I2CTM.

The EEPROM also provides an additional 64 byte identification page area. This area is used by DH electronics to store manufacturer specific information and cannot be used freely. But the normal EEPROM area can be used by the customer without any restrictions.

13 RTC

In addition to the RTC integrated in the STM32MP2, the DHCOS-STM32MP2-01LG is available with the optional onboard temperature compensated RTC RV-3032-C7 from Micro Crystal. The RTC is connected to the STM32MP2 I2C8 port. Please also have a look at chapter 15 On-Module I2CTM.

The additional RTC can be supplied during time keeping mode via a goldcap or a coin cell battery. Therefore, the supply voltage can be applied through the VRTC connection. Please have also a look at 13.1.2 VRTC.

Features:

- Factory calibrated temperature compensation
- Very high Time Accuracy (best in class).
  - ±1.5 ppm 0 to +50°C
  - ±3.0 ppm -40 to +85°C
- Low power consumption: 160 nA @ 3 V.
- Wide operating voltage range: 1.3 V to 5.5 V.
- Aging compensation with OFFSET value
- Counters for hundredths of seconds, seconds, minutes, hours, date, month, year and weekday

Note: The low active INT pin of the RTC is connected to the PI10 port of the STM32MP2.

13.1 VBAT and VRTC: Backup voltage buffering

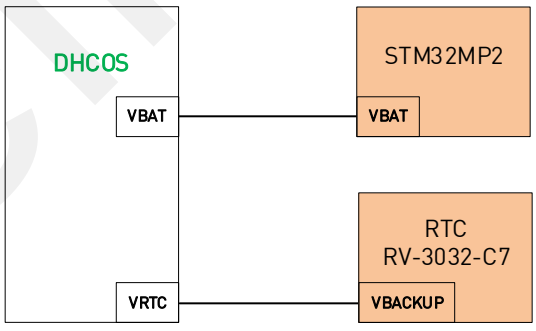


Figure 12: VRTC and VBAT supply

13.1.1 VBAT

The STM32MP2 real-time clock (RTC) and backup registers can be supplied with the VBAT voltage when the main VOUT = VIO supply is powered off. This internal supply with automatic switch between VBAT and VOUT = VIO is named VSW domain and is also used to supply PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6 pads.

If no external battery is used in the application, it is required to connect VBAT externally to VOUT = VIO.

13.1.2 VRTC

When ordering the DHCOS-STM32MP2-01LG with the option [-RTC], VRTC is connected to the additional RTC RV-3032-C7 to apply the needed backup voltage from carrier board.

If backup buffering of the additional RTC is not needed, the VRTC pin can be left open. In that case, the RTC is only supplied via VOUT = VIO and the RTC loses time and date information when the power is switched off.

Please refer to the technical documentation for details: https://www.microcrystal.com/en/products/real-time-clock-rtc-modules/rv-3032-c7/

14 ADC / DAC reference voltage

The PMIC Buck5 (1.8 V by default) is connected as external reference voltage, to the V_{REF+} pin of the STM32MP2 CPU. If an external reference voltage is required, please contact DH electronics for a special variant of the DHCOS-STM32MP2-01LG.

15 On-Module I2C™

The DHCOS-STM32MP2-01LG uses two I2C™ interfaces on the System on Module to connect different peripheral devices. The I2C4 port of the STM32MP2 is only connected to the PMIC and the interface is not accessible from the outside. In contrast, the STM32MP2 I2C8 port is used on the SOM and is also connected to the DHCOS I2C1 interface. This means that the DHCOS I2C1 port must be checked for collisions during the mainboard design. The third I2C interface is the STM32MP2 I2C2, which is only connected to the DHCOS I2C0 interface. This interface is not connected to any devices on the System on Module.

Note: For all three I2C devices pull-up resistors (1k5) to VIO are located at the DHCOS module.

15.1 PMIC I2C / STM32MP2 I2C4™

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2C4_SCL	I²C-bus clock (pull-up on the SOM)	PA12	VIO	-	GPIO	I/O
I2C4_SDA	I²C-bus data (pull-up on the SOM)	PD10	VIO	-	GPIO	I/O

Table 40: I2C4™ interface signals

Device		Address (7bit)
PMIC	ST STPMIC25DPQR	0x33

Table 41: I2C4™ connected devices

15.2 DHCOS I2C0 / STM32MP2 I2C2™

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2C2_SCL	I²C-bus clock (pull-up on the SOM)	PB5	VIO	-	GPIO	I/O
I2C2_SDA	I²C-bus data (pull-up on the SOM)	PB4	VIO	-	GPIO	I/O

Table 42: I2C2™ interface signals

15.3 DHCOS I2C1 / STM32MP2 I2C8™

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
I2C8_SCL	I²C-bus clock (pull-up on the SOM)	PZ4	VIO	-	GPIO	I/O
I2C8_SDA	I²C-bus data (pull-up on the SOM)	PZ9	VIO	-	GPIO	I/O

Table 43: I2C8™ interface signals

Device		Address (7bit)
IO-Expander	KTS1622EUAA	0x20
EEPROM (Memory)	M24256E	0x50
EEPROM (ID page)	M24256E	0x58
RTC	RV-3032-C7	0x51
Temperature sensor	TMP110D	0x40

Table 44: I2C8™ connected devices

16 Wi-Fi® / Bluetooth

The DHCOS-STM32MP2-01LG module is available with the optional onboard Wi-Fi® and Bluetooth module Type 2FY from muRata. Wi-Fi® is connected to the 4-bit SDMMC3 interface of the STM32MP2 SoC and Bluetooth® to UART8.

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
SDMMC3_CK	Clock output	PB13	VIO	N7	GPIO	O
SDMMC3_CMD	Command signal	PD12	VIO	P7	GPIO	I/O
SDMMC3_D0	Data signal bit 0	PB14	VIO	R7	GPIO	I/O
SDMMC3_D1	Data signal bit 1	PD13	VIO	T7	GPIO	I/O
SDMMC3_D2	Data signal bit 2	PB12	VIO	U7	GPIO	I/O
SDMMC3_D3	Data signal bit 3	PD14	VIO	V7	GPIO	I/O

Table 45: SDMMC3 interface signals

Note: The listed STM32MP2 SDMMC3 pins are only externally available on DHCOS SDIO1 when using a SOM without the -WBT option.

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
UART8_TX	UART1 TX transmit data output	PI11	VIO	-	GPIO	O
UART8_RX	UART1 RX receive data input	PF11	VIO	-	GPIO	I
UART8_RTS	UART1 request to send	PB15	VIO	-	GPIO	O
UART8_CTS	UART1 clear to send	PH5	VIO	-	GPIO	I

Table 46: UART8 interface signals

STM32MP2 function	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
WL_REG_ON	WiFi section power-up GPIO → Connected to IO-Expander (I2C: 0x20; P0.3)	-	VIO	-	GPIO	O
BT_REG_ON	Bluetooth section power-up GPIO → Connected to IO-Expander (I2C: 0x20; P0.2)	-	VIO	-	GPIO	O
SOC_SF5 = VWBT_32k	WiFi/BT 32kHz clock reference voltage 1V8 output voltage → Connected to PMIC: BUCK5	-	1V8	T8	GPIO	O
SOC_SF20	WL_HOST_WAKE WiFi host wake output → Connected to muRata 2FY pin 2 (GPIO_0/WL_HOST_WAKE)	-	1V8	Y21	GPIO	O
SOC_SF21	BT_HOST_WAKE Bluetooth host wake output → Connected to muRata 2FY pin 41 (BT_HOST_WAKE)	-	1V8	Y22	GPIO	O
SOC_SF22	WL_DEV_WAKE WiFi device wake input → Connected to muRata 2FY pin 5 (GPIO_1/ LHL)	-	1V8	R4	GPIO	I

Table 47: Additional WiFi/BT signals

Note: The SOC_SF5 = VWBT_32k is also used as reference voltage for the external needed WBT_32kHz_REFCLK clock source (connected to DHCOS pin A6). For the DHCOS-STM32MP2-01LG the 32kHz clock must be supplied by 1V8.

The muRata 2FY uses the Infineon CYW55513 chipset and offers tri band 2.4GHz, 5 GHz and 6 GHz Wi-Fi® and Bluetooth® v5.4 support.

16.1 Features

Wi-Fi®:

- Compliant with IEEE802.11a/b/g/n/ac/ax
- Data rate on Wi-fi® PHY up to 143Mbps
- Tri band 2.4 GHz, 5 GHz and 6 GHz support
- STA and SoftAP mode

Bluetooth®:

- Bluetooth® 5.4 BR/EDR/LE
- Data rate on Bluetooth® PHY up to 3Mbps

16.2 32kHz reference clock

The DHCOS Pin A6 WBT_32kHz_REFCLK is connected to the WiFi/BT module 2FY LPO_IN Pin 30. This pin must be connected to an external 32kHz oscillator, if the WiFi/BT module 2FY is mounted on the System on Module. For more information see muRata 2FY datasheet.

The SOC_SF5 = VWBT_32k pin can be used as reference voltage for the external needed WBT_32kHz_REFCLK clock source (connected to DHCOS pin A6). For the DHCOS-STM32MP2-01LG the 32kHz clock must be supplied by 1V8.

16.3 Antenna and connector

On the DHCOS-STM32MP2-01LG a standard U.FL. connector from TE 1909763-1 is used. U.FL. is compatible with the IPEX MHF1 connector specification.

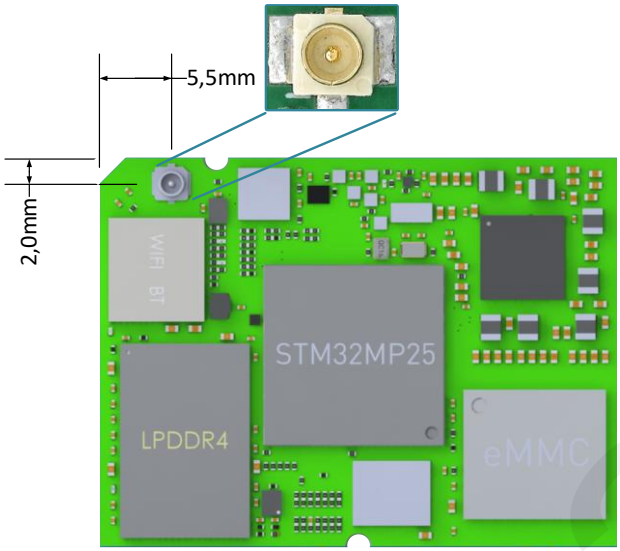


Figure 13: Wi-Fi/BT U.FL. connector

Murata recommends the following external antenna:

Unictron WT32D1-KX - H2B1WD1A3B0200

Figure 14: Unictron WT32D1-KX

Characteristics:

- Dimension (mm): 32.0 x 13.0 x 0.5
- Cable and Connector: L=130mm/IPEX I
- Frequency (MHz): 2400 ~ 2500, 5150 ~ 5850, 5925 ~ 7125
- Polarization: Linear
  - 2400 ~ 2500 MHz
    Peak Gain (dBi): 3 Max (Typical)
    VSWR: 2 Max. (Typical)
  - 5150 ~ 5850 MHz
    Peak Gain (dBi): 5.2 Max (Typical)

VSWR: 2 Max. (Typical)

- 5925 ~ 7125 MHz
  Peak Gain (dBi): 4 Max (Typical)
  VSWR: 2 Max. (Typical)

- 119mm long cable and IPEX MHF I connector
- -10°C to +85°C
- Humidity 10% to 70% RH

17 Ethernet connection

17.1 1Gbit Ethernet (DHSBC board configuration)

The DHSBC STM32MP2x board (see 4.3 Reference design: DHSBC STM32MP2x (DH Single Board Computer)) implements dual 1Gbit Ethernet connection.

For signal description, please have a look at 4.4.19.1 ETH0 and 4.4.19.2 ETH1.

17.2 100Mbit Ethernet

REFCLK Notes:

- 50 MHz REFCLK is required in RMII.
- Either the MAC or PHY can supply it, but not both. → **DHCOS only supports the PHY providing the REF-CLK to the MAC.**
- The clock must be shared between the MAC and PHY for proper operation.

Supported REFCLK path: PHY provides REFCLK (Most common)

- The PHY has an onboard oscillator or uses an external crystal to generate 50 MHz.
- The 50 MHz clock is output from the PHY to the MAC.
- Most RMII-compatible PHYs support this mode.

This chapter shows how to connect two 100MBit PHY's to the DHCOS-STM32MP2-01LG:

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ETH0_TX_CTL	ETH0_RMII_TX_EN = Transmit data enable	PA13	VRGMII	A7	GPIO	O
ETH0_TD0	Transmit data bit 0	PA15	VRGMII	A11	GPIO	O
ETH0_TD1	Transmit data bit 1	PC1	VRGMII	A10	GPIO	O
ETH0_RX_CTL	ETH0_RMII_CRS_DV = Carrier Sense (CRS) and RX_Data Valid (RX_DV)	PA11	VRGMII	A13	GPIO	I
ETH0_RD0	Receive data bit 0	PF1	VRGMII	A17	GPIO	I
ETH0_RD1	Receive data bit 1	PC2	VRGMII	A16	GPIO	I
#ETH0_RST	Ethernet PHY reset (active low) → Connected to IO-Expander (I2C: 0x20; P0.1)	-	VIO	A19	GPIO	O
ETH0_INT	Ethernet PHY interrupt (active high)	PC6	VIO	A20	GPIO	I
ETH0_RXC	ETH0_RMII_REF_CLK = RMII 50 MHz reference clock	PA14	VRGMII	A18	GPIO	I
ETH0_MDIO	Management bus data signal	PF2	VRGMII	A22	GPIO	I/O
ETH0_MDC	Management bus clock signal	PF0	VRGMII	A23	GPIO	O
ETH1_TX_CTL	ETH1_RMII_TX_EN = Transmit data enable	PC4	VRGMII	AA7	GPIO	O

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ETH1_TD0	Transmit data bit 0	PC7	VRGMII	AA11	GPIO	O
ETH1_TD1	Transmit data bit 1	PC8	VRGMII	AA10	GPIO	O
ETH1_RX_CTL	ETH1_RMII_CRS_DV = Carrier Sense (CRS) and RX_Data Valid (RX_DV)	PC3	VRGMII	AA13	GPIO	I
ETH1_RD0	Receive data bit 0	PG0	VRGMII	AA17	GPIO	I
ETH1_RD1	Receive data bit 1	PC12	VRGMII	AA16	GPIO	I
#ETH1_RST	Ethernet PHY reset (active low) → Connected to IO-Expander (I2C: 0x20; P0.0)	-	VIO	AA19	GPIO	O
ETH1_INT	Ethernet PHY interrupt (active high)	PG3	VIO	AA20	GPIO	I
ETH1_RXC	ETH1_RMII_REF_CLK = RMII 50 MHz reference clock	PF6	VRGMII	AA18	GPIO	I
ETH1_MDIO	Management bus data signal	PC5	VRGMII	AA22	GPIO	I/O
ETH1_MDC	Management bus clock signal	PG4	VRGMII	AA23	GPIO	O

Table 48: Ethernet 100Mbit RMII signals

Notes:

- ETH*_REFCLK is not supported in RMII = 100MBit Ethernet mode.
- ETH0_RMII_REF_CLK input is available on ETH0_RXC (MP2 Port: PA14) and ETH1_RMII_REF_CLK input on ETH1_RXC (MP2 Port: PF6), but using these inputs as a 50MHz reference will cause your design to break the DHCOS standard. With RMII mode it is recommended to use the internal 50MHz reference clock.

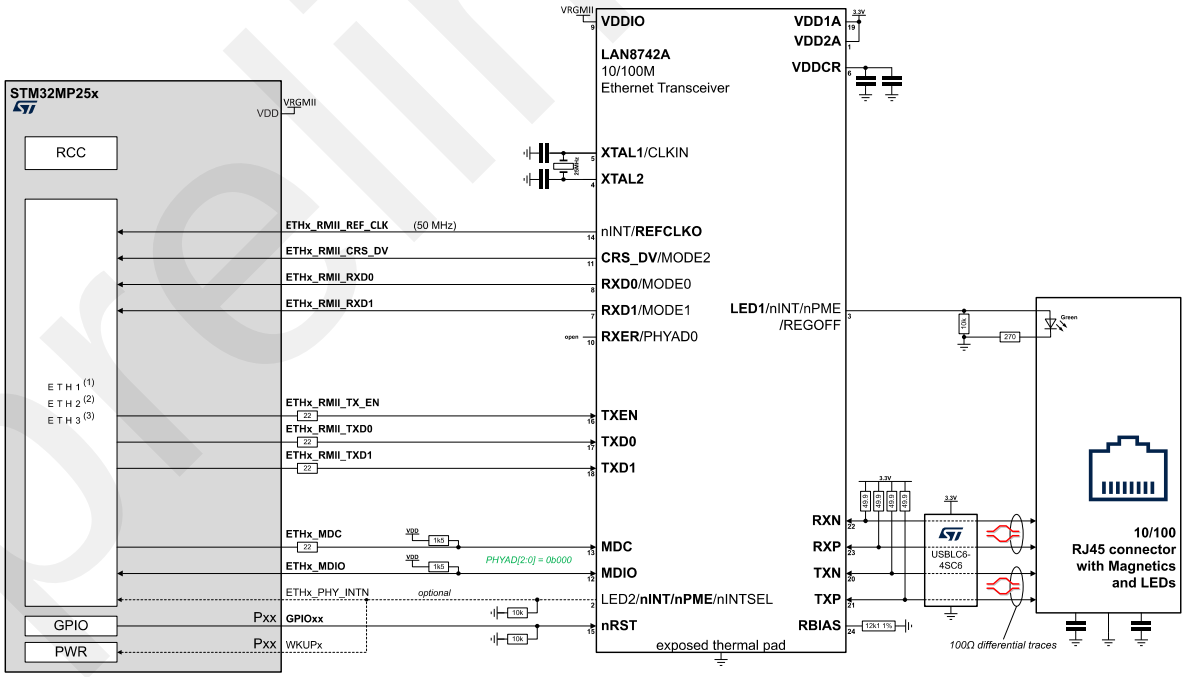


Figure 15: Ethernet 100Mbit example with PHY LAN8742A

17.3 Ethernet port 3

Tbd..

18 Display connection

The DHCOS-STM32MP2-01LG provides a native 18-bit parallel digital RGB (Red, Green, Blue) interface, 2x link LVDS and 4x lane MIPI DSI® with the following features:

- Optional 3D GPU: VeriSilicon® - Up to 900 MHz
  - OpenGL® ES 3.1 - Vulkan 1.3
  - OpenCL™ 3.0, OpenVX™ 1.3
  - Up to 150 Mtriangle/s, 900 Mpixel/s
- LCD-TFT controller, up to 24-bit // RGB888
  - Up to FHD (1920 × 1080) @60 fps
  - 3 layers including a secure layer
  - YUV support, 90° output rotation
- MIPI DSI®, 4× data lanes, up to 2.5 Gbit/s each
  - Up to QXGA (2048 × 1536) @60 fps
- FPD-1 and OpenLDI JEIDA/VESA (LVDS), up to 2× links of 4× data lanes, up to 1.1 Gbit/s per lane
  - Up to QXGA (2048 × 1536) @60 fps

18.1 Missing RGB signals for 24bit support

Notes:

- With DHCOS-STM32MP2-01LG standard System on Module only 18-bit is supported. 24-bit can be realized if no second Ethernet interface is required, but then compatibility with DHCOS standard is lost.
- The 18-bit RGB output is only available when the -RGB option is selected. However, this means that the DHCOS UART interfaces UART2 and UART3 are no longer available.
- It is recommended to use an LVDS-to-RGB bridge instead.

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
ETH1_TX_CTL	MP2 function LCD_R0 = Red data bit 0	PC4	VRGB	AA7	GPIO	O
ETH1_TXC	MP2 function LCD_R1 = Red data bit 1	PF7	VRGB	AA12	GPIO	O
ETH1_REFCLK	MP2 function LCD_G0 = Green data bit 0	PF8	VRGB	AA21	GPIO	O
ETH1_RD1	MP2 function LCD_G1 = Green data bit 1	PC12	VRGB	AA16	GPIO	O
ETH1_RXC	MP2 function LCD_B0 = Blue data bit 0	PF6	VRGB	AA18	GPIO	O
GPIO_L	MP2 function LCD_B1 = Blue data bit 1	PA3	VRGB	V28	GPIO	O

Table 49: Missing 24bit RGB signals

19 Hardware and DDR3 coding

Notes:

- Some of the 24-bit RGB signals are used on the SOM for DDR memory and PCB hardware coding.
- In parallel display usage, the 10k pull-up or pull-down resistor does not cause any issues with the RGB signal.
- The bootloader reads the signal state during the initial boot stages. Later, these signals can be used for a parallel display.
- Ensure that the mainboard design does not modify the logic level of the pins at system boot, because the bootloader (U-Boot) scans the states of these pins during startup, starts the correct memory initialization and provides information regarding the PCB version in order to handle possible PCB differences correctly.

The following pins are used by DH electronics for hardware and DDR3 size coding:

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
RGB_R4	RAM-CODE_2	PF15	VRGB	J7	GPIO	I
RGB_G4	RAM-CODE_1	PG10	VRGB	J6	GPIO	I
RGB_G3	RAM-CODE_0	PG9	VRGB	H6	GPIO	I
RGB_B4	HW-CODE_2	PI1	VRGB	H5	GPIO	I
RGB_B3	HW-CODE_1	PI0	VRGB	G5	GPIO	I
RGB_B2	HW-CODE_0	PG15	VRGB	F5	GPIO	I

Table 50: Hardware and DDR coding pins

Hardware (PCB) version	PI1: HW Code bit 2	PI0: HW Code bit 1	PG15: HW Code bit 0
HW100 (version 1)	0	0	0
HW200 (version 2)	0	0	1
HW300 (version 3)	0	1	0
HW400 (version 4)	0	1	1
...			
HW800 (version 8)	1	1	1

Table 51: Hardware coding

LPDDR4 size	PF15: RAM Code bit 2	PG10: RAM Code bit 1	PG9: RAM Code bit 0
512 MByte	0	0	0
1 GByte	0	0	1
reserved	0	1	0
2 Gbyte	0	1	1
3 Gbyte	1	0	0
4 Gbyte	1	0	1
reserved	1	1	0
reserved	1	1	1

Table 52: LPDDR4 coding

Note:

- 1 = 10k pull-up at DHCOS module
- 0 = 10k pull-down at DHCOS module

19.1 Mainboard hardware coding

DHCOS pad name	Description / Notes	CPU pin name	Voltage level	DHCOS pad number	Ball Type	I/O Type
GPIO_M	Mainboard HW-CODE_2	PA1	VIO	L27	GPIO	I/O
GPIO_L	Mainboard HW-CODE_1	PA3	VIO	V28	GPIO	I/O
GPIO_K	Mainboard HW-CODE_0	PA2	VIO	U28	GPIO	I/O

Table 53: Mainboard coding pins

Mainboard-HW (PCB) version	PA1: HW Code bit 2	PA3: HW Code bit 1	PA2: HW Code bit 0
HW100 (version 1)	0	0	0
HW200 (version 2)	0	0	1
HW300 (version 3)	0	1	0
HW400 (version 4)	0	1	1
…			
HW800 (version 8)	1	1	1

Table 54: Mainboard-HW coding on DHSBC board

Notes:

- 1 = A 10k pull-up should be placed on the mainboard to allow the coding to be used in dedicated customer projects.
- 0 = A 10k pull-down should be placed on the motherboard to allow the coding to be used in dedicated customer projects.
- If a customer wishes to implement the hardware coding option on their mainboard, it is recommended that the GPIOs K–M are reused, as the scan output is already implemented in the DHSBC reference design. If no hardware coding is needed for the mainboard, the pins can be used as standard GPIOs. However, the scan out must be removed from the bootloader (U-Boot).

20 JTAG / SWD connection

For signal description, please have a look at 4.4.3 JTAG.

To avoid uncontrolled, I/O levels the STM32MP2 series embeds internal pull-up and pull-down resistors on the JTAG pins:

- SYS_JTRST: Internal pull-up
- SYS_JTDI: Internal pull-up
- SYS_JTDO-SWO: Internal pull-up
- SYS_JTMS-SWDIO: Internal pull-up
- SYS_JTCK-SWCLK: Internal pull-down
- The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST but there is no special recommendation for TCK. However, for the lines, an integrated pull-down resistor is used for JTCK.
- Having embedded pull-up and pull-down resistors removes the need to add external resistors.
- In order to use the RMA (return material acceptance), the JTAG pins (JTDI, JTCK, JTMS) must be accessible. The JTDO pin might be needed too, depending on the tool that is used.

The next figure shows the connection between the STM32MP2 series and a standard JTAG/SWD connector:

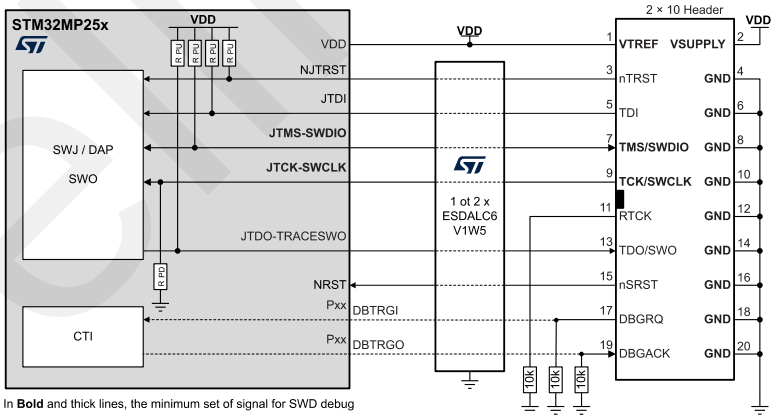


Figure 16: JTAG / SWD Connection

21 UART for bootloader and Linux console

DHCOS UART0 is reserved to enable access to the bootloader and linux console on the carrier board. The port can be deactivated during production to avoid illegal access to the series device, but for development and prototyping this port should be accessible.

For signal description, please have a look at 4.4.4.1 UART0.

22 USB boot and flash programming

It is strongly recommended to enable the access to the DHCOS USB0 port on the carrier board and the possibility to switch to USB boot mode. Then the standard Linux dfu-util can be used to start up the board and the dfu or ums bootloader utils can be used to program any flash device supported on STM32MPU boards:

- microSD™ card
- eMMC
- NOR Flash memory

For signal description, please have a look at 4.4.20.1 USB0.

Notes:

- For USB booting, only the USB0_D- and USB0_D+ signals need to be connected.
- When USB0 is connected to a standard host port, an "illegal" A-to-A cable (without a VBUS connection) can be used during development or production to enable access to the device via USB.

23 Technical specifications

23.1 Operating conditions – Absolute maximum / operating conditions

Symbol	Description	Input / Output	Min	Typ	Max	Unit
VCC_IN	5V supply voltage	Input	4.2	5.0	5.5	V
P_{VCC_IN} [1]	Max. power consumption w/o WiFi/BT	Input	-	Tbd	See 23.2	W
	Max. power consumption with WiFi/BT	Input	-	Tbd	See 23.2	W
VCC_IN_{ripple}	VCC ripple peak-to-peak	Input	-	30	60	mV
VBAT	STM32MP2 Backup operating voltage	Input	2.3	-	3.6	V
I_{VBAT}	Max. backup current	Input	-	-	6.1	µA
VRTC	RTC backup supply voltage	Input	1.1	-	5.5	V
I_{VRTC}	Max. backup current	Input	-	160	180	nA
ADC_VREF	Analog reference voltage **Note: Must not be connected. Is supplied internally.**	Input	1.1	1.8	1.85	V
VOUT = VIO	IO voltage	Output	-	3.3	-	V
I_{VOUT} [2]	Max. usable VCC_IO output current (with WiFi/BT)	Output	-	-	1200	mA
VRGMII	RGMII output voltage	Output	-	3.3	-	V
I_{VRGMII}	Max. usable VRGMII output current	Output	-	-	100	mA
VSDIO0	SDIO0 output voltage	Output	-	1.8 or 3.3	-	V
I_{VSDIO0}	Max. usable VSDIO0 output current	Output	-	-	20	mA
VSDIO1	SDIO1 output voltage	Output	-	3.3	-	V
I_{VSDIO1}	Max. usable VSDIO1 output current	Output	-	-	20	mA
VRGB	RGB output voltage	Output	-	3.3	-	V
I_{VRGB1}	Max. usable VRGB output current	Output	-	-	20	mA
PMIC_BUCK5 = SOC_SF5 = VWBT_32k	Special function PMIC: BUCK5	Output	-	1.8	-	V
I_{PMIC_BUCK5}	Max. usable PMIC_BUCK5 output current	Output	-	-	150	mA
V_{IL}	I/O input low level voltage	Input	-	-	0.3x Voltage level	V
V_{IH}	I/O input high level voltage	Input	0.7x Voltage level	-	-	V

Table 55: DC operating conditions

Note: The carrier board designer MUST always consider the thermal conditions on the DHCOS module.

23.2 Absolute maximum power consumption

Symbol	Description	Power symbol	Max. power value
VDD_CORE	Digital core supply voltage	$P_{VDD\_CORE\_MAX}$	0.98 W (1200 mA @ 0.82 V @ 125°C)
VDD_CPU	ARM-core supply voltage	$P_{VDD\_CPU\_MAX}$	0.41 W (510 mA @ 0.8 V @ 125°C)
VDD_GPU	ARM-core supply voltage	$P_{VDD\_CPU\_MAX}$	0.33 W (390 mA @ 0.84 V @ 125°C)

[1] Only DHCOS STM32MP2 without any output power consumption.
[2] VOUT = VIO System on Module current consumption: PMIC = 150mA, IO-Expander = 160mA, WiFi/BT = 450mA → max. 310mA w/o WiFi/BT and 760mA with WiFi/BT

Symbol	Description	Power symbol	Max. power value
VDDQDDR	DDR supply voltage	$P_{VDDQDDR\_MAX}$	0.54 W (490 mA @ 1.1 V)
VDDIO	IO supply voltage	P_{VDDIO_MAX}	0.3 W
LPDDR4	LPDDR4 Burst Read	P_{LPDDR4_MAX}	1.8 W
eMMC	eMMC Read	P_{eMMC_MAX}	0.5 W
QSPI	QSPI Burst Read	P_{QSPI_MAX}	0.1 W
WiFi/BT	WiFi/BT max power consumption	P_{WiFi/BT_MAX}	1.5 W
Maximum power consumption DHCOS STM32MP2			**5.0 W** (w/o WiFi/BT) **6.50 W** (with WiFi/BT) [3]

Table 56: DHCOS STM32MP2 max. power consumption (only System on Module)

23.3 Reset Timings

Symbol	Description	Min	Typ	Max	Unit
#RST_IN	Internal pull-up resistor	18	-	36	kΩ
	System Reset input assertion time (active low)	0.02[4]	1	-	ms
#RST_OUT	Internal pull-up resistor	-	10	-	kΩ
	System Reset output power-cycle (active low)	-	25	-	ms

Table 57: Reset Timings

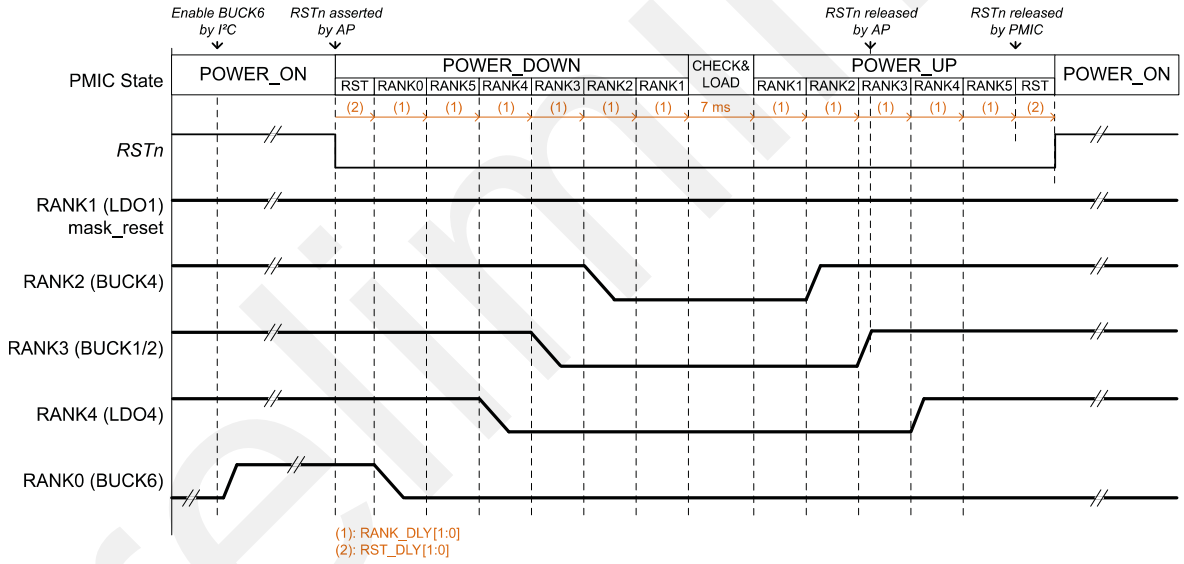


Figure 17: Reset Timings

Notes:

- Used PMIC is STPMIC25**D**: Default delays
  - RST_DLY = 0ms
  - RANK_DLY = 1.5ms

[3] Please include an adequate buffer in the power supply design.
[4] PMIC RSTnDB time

23.4 Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_AMB	Default operating temperature range	-25		85	°C

Table 58: Temperature range

Notes:

- Industrial temperature range for eMMC and LPDDR4 version is -25 °C - 85 °C. Please contact us for -40 °C - 85 °C version
- Please contact us commercial temperature range (0 °C - 70 °C)

24 Mechanical specifications

24.1 Dimensions

Please note that the **DHCOS-STM32MP2-01LG** comes in **M-size**. However, to ensure compatibility with other DHCOS System-on-Modules, it is recommended that the L-size land pattern is used when designing the carrier board.

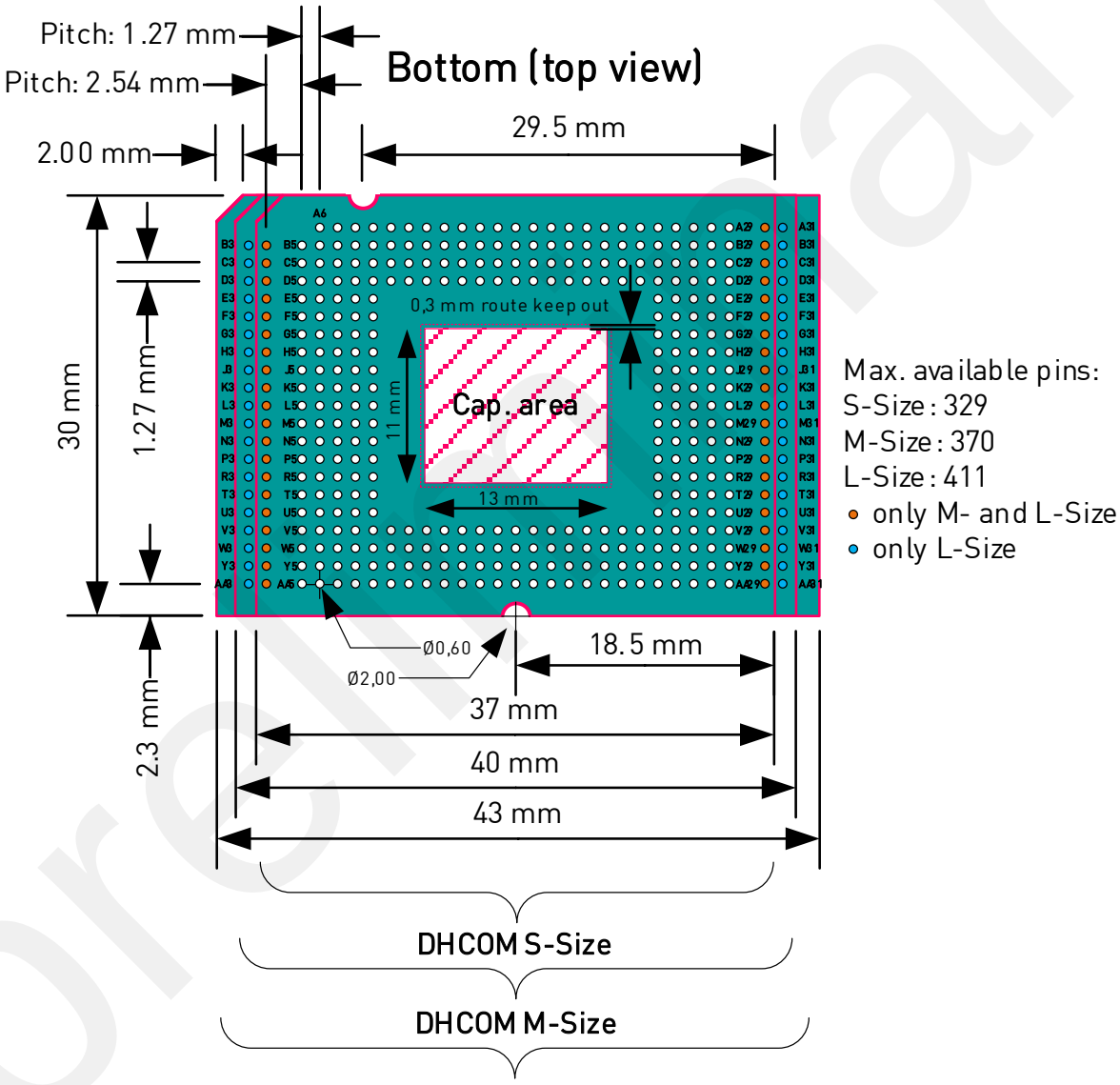


Figure 18: Dimensions of the module

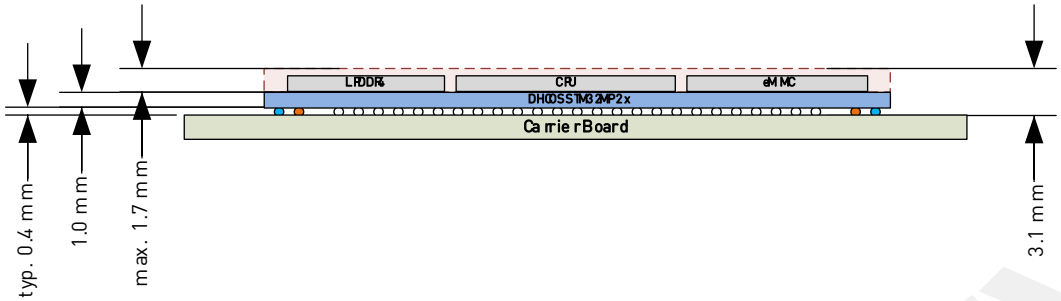


Figure 19: DHCOS height[5]

24.2 PCB land pattern

Important: The mainboard design requires a PCB cutout measuring 12 mm x 14 mm!

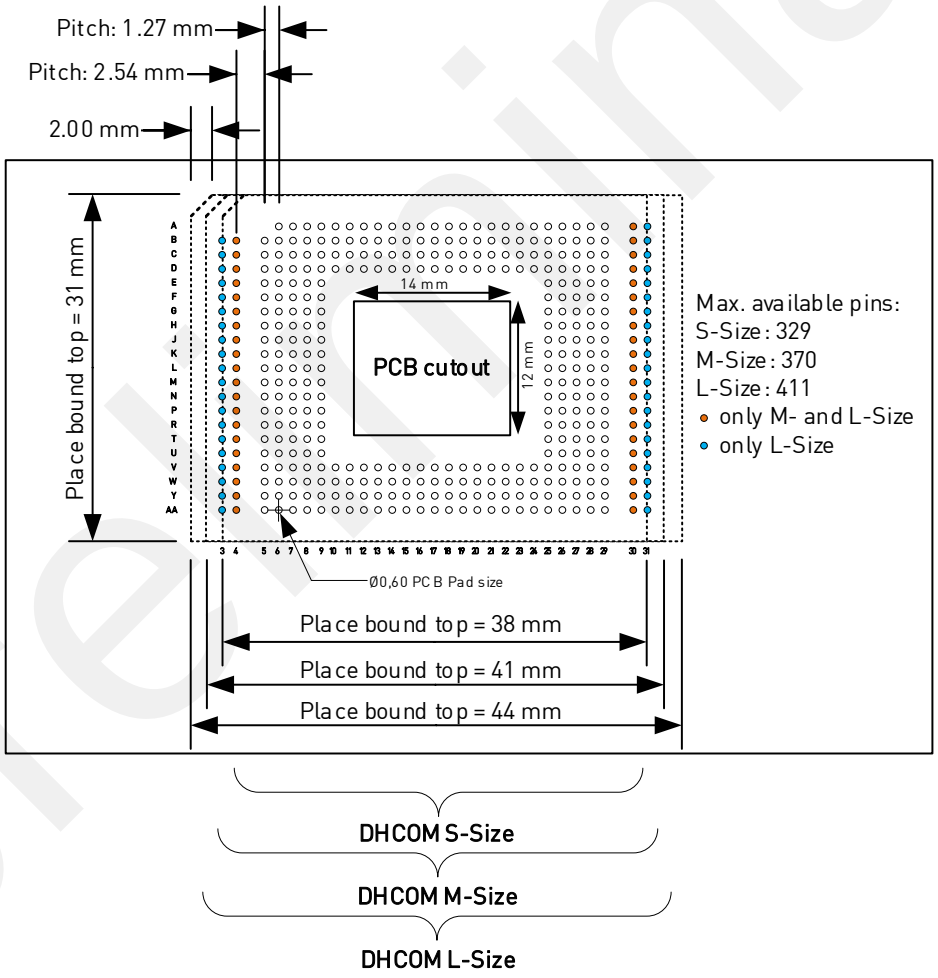


Figure 20: PCB land pattern

[5] Max. 3.1mm without U.FL connector counterpart.

25 Assembly instructions

DHCOS-STM32MP2-01LG has been designed for SMT mounting of the module on the carrier board. The DHCOS uses LGA contact pads on the bottom side for the connection to the carrier board. During the production process of the module solder paste is applied to the LGA pads. Therefore, the DHCOS is nearly similar to a BGA. The solder paste on the pads improves the contact quality between module and carrier board, compared with a standard LGA part (without solder paste on the module pads).

25.1 Moisture sensitivity and shelf life

- Calculated shelf life in tape and real packaging: 12 months at < 40 °C and < 90 % relative humidity (RH).
- The DHCOS-STM32MP2-01LG is applicable to MSL3 (based on IPC/JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at < 30 °C and < 60 % RH and the product shall be used within 168 hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 $^{+5}/_{-0}$ °C, 24 hours, 1 time
- The products shall be baked on a heat-resistant tray since the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

25.2 Coplanarity

Coplanarity of the carrier board: < 0.1 mm

25.3 Solder pastes

Solder paste parameters:

- Any lead-free (Pb-free) SAC solder pastes can be used.

Solder paste print parameters:

- Stencil thickness: > 0.1 mm (recommended 0.15 mm)
- Stencil pad diameter: Suggestion 0.55 mm (0.6 mm pad size)

25.4 Reflow Process

Use reflow profiles per IPC/JEDEC J-STD-020D.

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_L)	 150 °C 200 °C 60-120 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60-150 °C
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6°C/second max.
Time 25 °C to peak temperature	8 minutes max.

Table 59: Reflow profil per IPC/JEDEC J-STD-020E

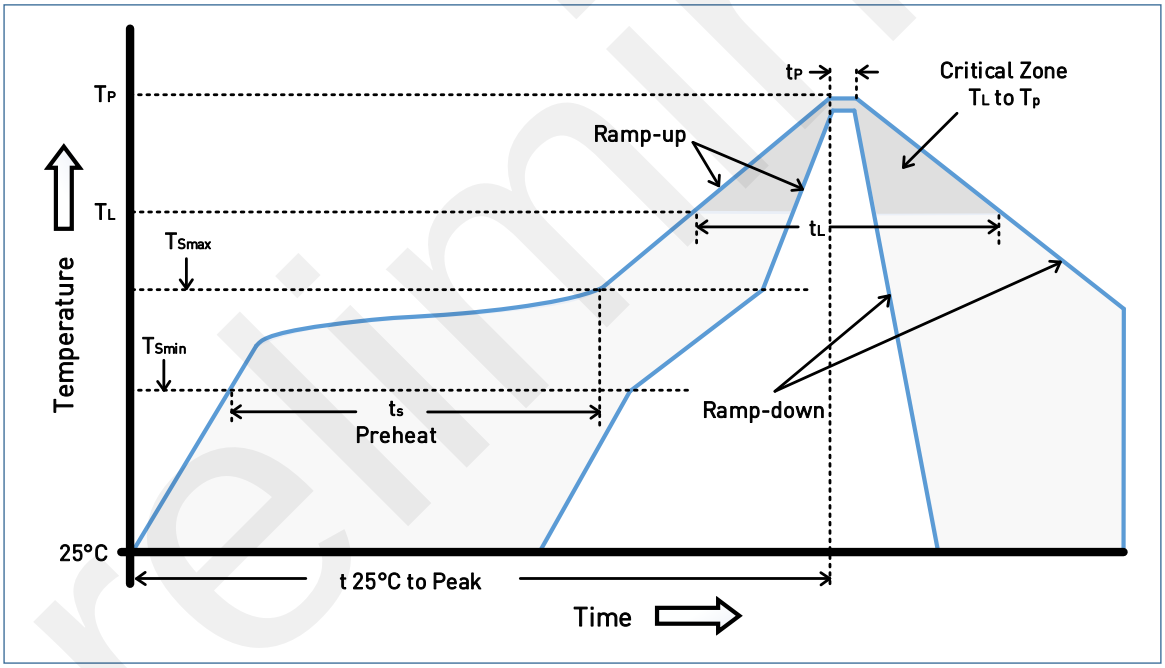


Figure 21: Reflow Classification Profile

The manufacturing of the DHCOS-STM32MP2-01LG requires two reflow cycles. Two reflow cycles are remaining for mounting the module on the carrier board. It is strongly recommended to solder the DHCOS-STM32MP2-01LG module during the last reflow cycle of the carrier board manufacturing process.

26 Tape and reel packaging

The DHCOS-STM32MP2-01LG comes in tape-and-reel packaging. The minimum order quantity (MOQ) is 360.

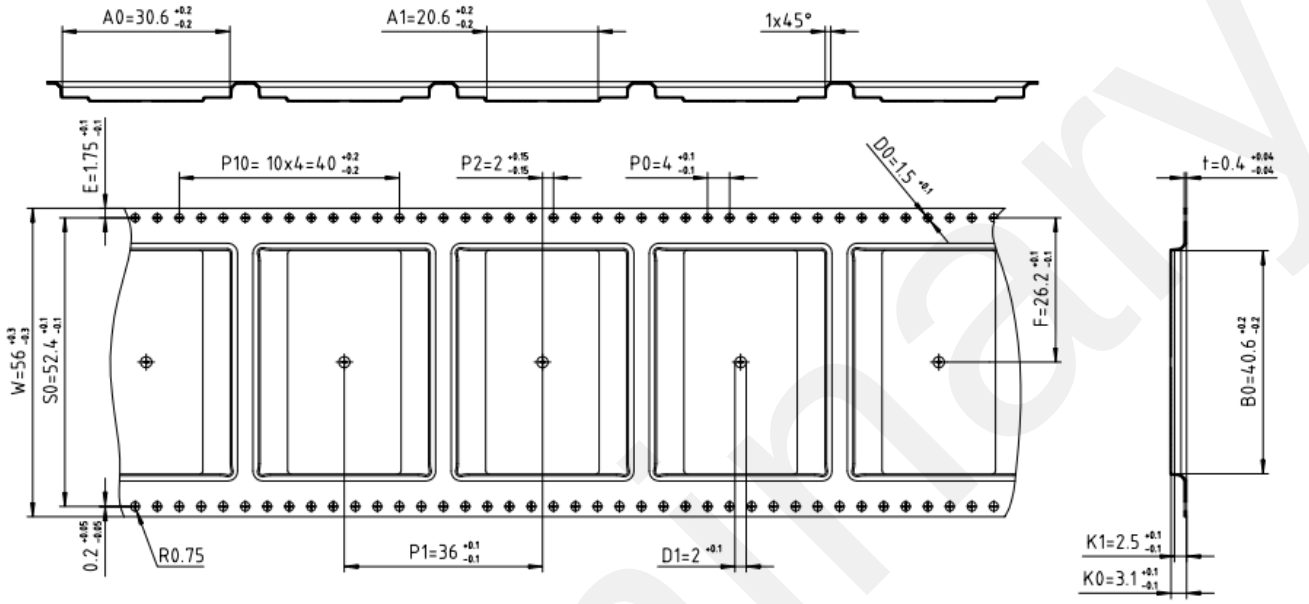


Figure 22: Tape and reel packaging

27 Hardware design checklist

Table 60 is a checklist for all the important design guidelines. Please read each checklist entry carefully to ensure that your carrier board design meets these guidelines.

Number	Checklist / Design notes
1	Does the carrier board design provide any connection to the JTAG pins (e.g. mounting option, only for development)? Please have a look at chapter 20 JTAG / SWD connection
2	Are the BOOT pins provided with correct pull-up or pull-down resistors for the preferred boot options? Please have a look at chapter 8 Boot modes
3	If a DHCOS variant with WiFi/BT is used, it is mandatory to connect WBT_32kHz_REFCLK pin on the carrier board design in the correct way. Please have a look at chapter 16.2 32kHz reference clock
4	DH electronics strongly recommends to enable the access to the USB0_D+ and USB0_D- lines to support the USB boot. Please have a look at chapter 22 USB boot and flash programming
5	Please provide a 0.1µF buffer capacitor at #RST_IN. Please have a look at chapter 7 Reset
6	Does the carrier board design provide any serial connection to bootloader and Linux console? Please have a look at chapter 21 UART for bootloader and Linux console
7	If this is needed, it is recommended that you reuse the Mainboard-HW coding pins for your customer-specific mainboard PCB coding. This means that no BSP adjustments are required. Please have a look at Table 53: Mainboard coding pins
8	Please ensure that your mainboard PCB design does not affect the state of the RAM-CODE_* and HW-CODE_* pins. Otherwise, the bootloader will read the wrong configuration. Please have a look at Table 51: Hardware coding and Table 52: LPDDR4 coding
9	SD Card connection: If a speed grade higher than "High Speed" (50 MHz) is required for an SD card, please use the SDIO0 interface instead of the SDIO1 interface. With SDIO0, the LDO8 of the PMIC provides the interface with a dedicated reference voltage, meaning the pins can be changed to 1.8 V IO during operation to support UHS-I mode. Additionally, the bootloader can be started directly from the SDIO0, meaning the system can be

Number	Checklist / Design notes
	started entirely from the SD card.
10	Please note that a REFCLK connection is needed between the CPU and the PHY in 100 Mbit Ethernet mode. Compatibility between different DHCOS System on Modules is not guaranteed for the 100Mbit connection. For 100% compatibility, please use a 1 Gbit Ethernet connection. Please have a look at 17 Ethernet connection
11	When designing the mainboard, make sure that there are no address collisions for DHCOS I2C1, as some devices are already connected to this port on the System on Module. Please have a look at 15.3 DHCOS I2C1 / STM32MP2 I2C8™
12	It is not possible to assign DHCOS I2C1 to the Cortex-M33 core because devices are already connected to this port on the system module. These devices must be managed by the Linux system. Please have a look at 15.3 DHCOS I2C1 / STM32MP2 I2C8™

Table 60: Hardware design checklist

28 RoHS conformance

This device has been manufactured RoHS II-compliant.

29 IPC class

The System on Module is manufactured to IPC Class 2 standards. For IPC class 3 support, please contact us.